PCF8574; PCF8574A

Remote 8-bit I/O expander for I²C-bus with interrupt

Rev. 5 — 27 May 2013 Product data sheet

1. General description

The PCF8574/74A provides general-purpose remote I/O expansion via the two-wire bidirectional I²C-bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 100 kHz I²C-bus interface, three hardware address inputs and interrupt output operating between 2.5 V and 6 V. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. System master can read from the input port or write to the output port through a single register.

The low current consumption of 2.5 μA (typical, static) is great for mobile applications and the latched output ports directly drive LEDs.

The PCF8574 and PCF8574A are identical, except for the different fixed portion of the slave address. The three hardware address pins allow eight of each device to be on the same I²C-bus, so there can be up to 16 of these I/O expanders PCF8574/74A together on the same I²C-bus, supporting up to 128 I/Os (for example, 128 LEDs).

The active LOW open-drain interrupt output ($\overline{INT}$) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I²C-bus.

The internal Power-On Reset (POR) initializes the I/Os as inputs with a weak internal pull-up 100 μA current source.

2. Features and benefits

- I²C-bus to parallel port expander
- 100 kHz I²C-bus interface (Standard-mode I²C-bus)
- Operating supply voltage 2.5 V to 6 V with non-overvoltage tolerant I/O held to V_{DD} with 100 μA current source
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs directly drive LEDs
- Total package sink capability of 80 mA
- Active LOW open-drain interrupt output
- Eight programmable slave addresses using three address pins
- Low standby current (2.5 μA typical)
- –40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: DIP16, SO16, SSOP20

3. Applications

- LED signs and displays
- Servers
- Key pads
- Industrial control
- Medical equipment
- PLC
- Cellular telephones
- Mobile devices
- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCF8574P	PCF8574P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCF8574AP	PCF8574AP			
PCF8574T/3	PCF8574T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574AT/3	PCF8574AT			
PCF8574TS/3	8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
PCF8574ATS/3	8574A			

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCF8574P	PCF8574P,112	DIP16	Standard marking * IC's tube - DSC bulk pack	1000	T_{amb} = −40 °C to +85 °C
PCF8574AP	PCF8574AP,112	DIP16	Standard marking * IC's tube - DSC bulk pack	1000	T_{amb} = −40 °C to +85 °C
PCF8574T/3	PCF8574T/3,512	SO16	Standard marking * tube dry pack	1920	T_{amb} = −40 °C to +85 °C
	PCF8574T/3,518	SO16	Reel 13" Q1/T1 *standard mark SMD dry pack	1000	T_{amb} = −40 °C to +85 °C
PCF8574AT/3	PCF8574AT/3,512	SO16	Standard marking * tube dry pack	1920	T_{amb} = −40 °C to +85 °C
	PCF8574AT/3,518	SO16	Reel 13" Q1/T1 *standard mark SMD dry pack	1000	T_{amb} = −40 °C to +85 °C

Table 2. Ordering options ...continued

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCF8574TS/3	PCF8574TS/3,112	SSOP20	Standard marking * IC's tube - DSC bulk pack	1350	T_{amb} = –40 °C to +85 °C
	PCF8574TS/3,118	SSOP20	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
PCF8574ATS/3	PCF8574ATS/3,118	SSOP20	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C

5. Block diagram

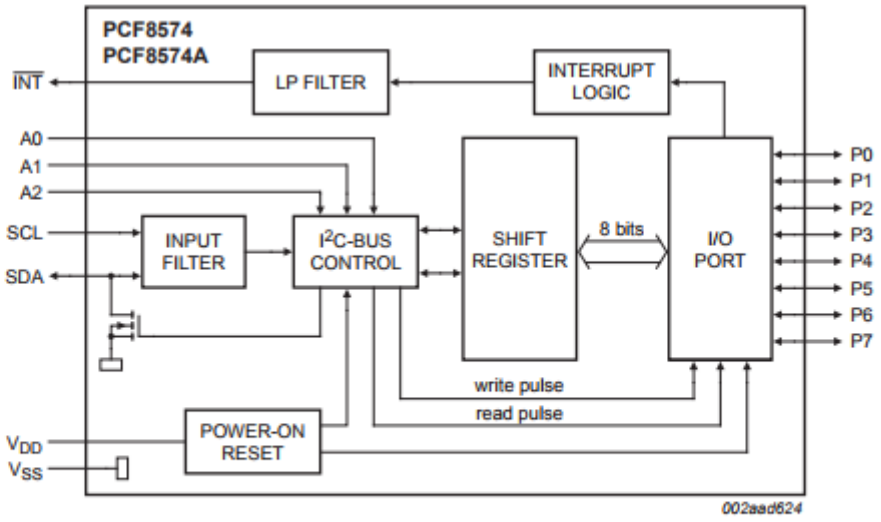


Fig 1. Block diagram

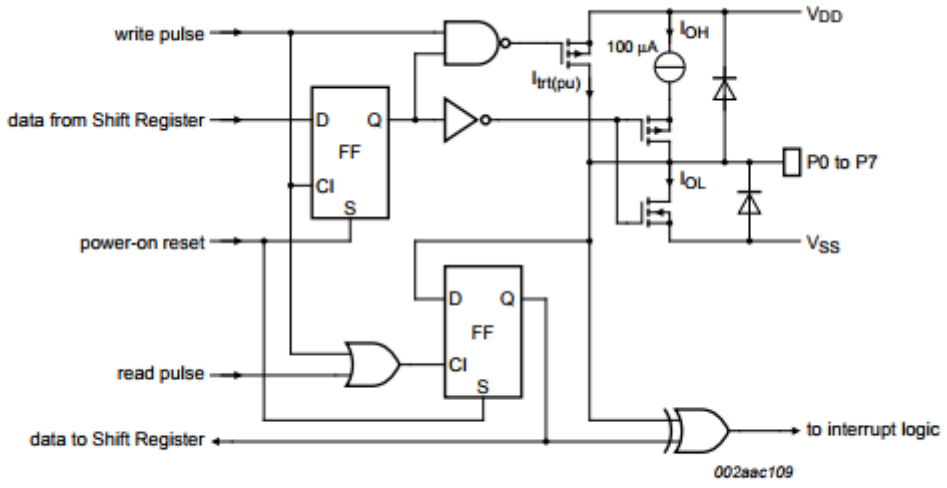


Fig 2. Simplified schematic diagram of P0 to P7

6. Pinning information

6.1 Pinning

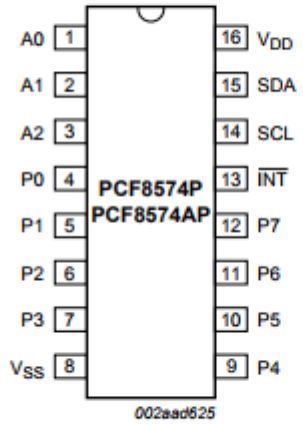


Fig 3. Pin configuration for DIP16

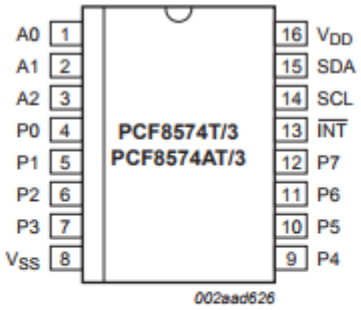


Fig 4. Pin configuration for SO16

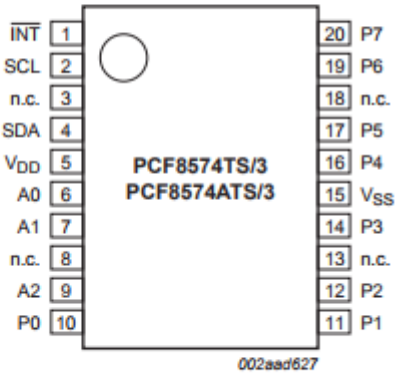


Fig 5. Pin configuration for SSOP20

6.2 Pin description

Table 3. Pin description

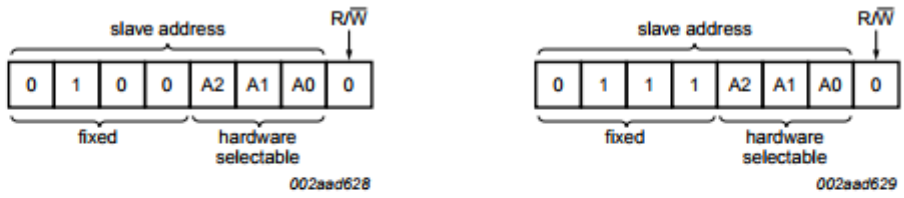
Symbol	Pin		Description
	DIP16, SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	-	3, 8, 13, 18	not connected

7. Functional description

Refer to Figure 1 “Block diagram”.

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address format of the PCF8574/74A is shown in Figure 6. Slave address pins A2, A1 and A0 are held HIGH or LOW to choose one of eight slave addresses. To conserve power, no internal pull-up resistors are incorporated on A2, A1 or A0, so they must be externally held HIGH or LOW. The address pins (A2, A1, A0) can connect to V_{DD} or V_{SS} directly or through resistors.



a. PCF8574 b. PCF8574A

Fig 6. PCF8574 and PCF8574A slave addresses

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation (write operation is shown in Figure 6).

7.1.1 Address maps

The PCF8574 and PCF8574A are functionally the same, but have a different fixed portion (A6 to A3) of the slave address. This allows eight of the PCF8574 and eight of the PCF8574A to be on the same I^2C-bus without address conflict.

Table 4. PCF8574 address map

Pin connectivity			Address of PCF8574								Address byte value		7-bit hexadecimal address without R/W
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{SS}	V_{SS}	V_{SS}	0	1	0	0	0	0	0	-	40h	41h	20h
V_{SS}	V_{SS}	V_{DD}	0	1	0	0	0	0	1	-	42h	43h	21h
V_{SS}	V_{DD}	V_{SS}	0	1	0	0	0	1	0	-	44h	45h	22h
V_{SS}	V_{DD}	V_{DD}	0	1	0	0	0	1	1	-	46h	47h	23h
V_{DD}	V_{SS}	V_{SS}	0	1	0	0	1	0	0	-	48h	49h	24h
V_{DD}	V_{SS}	V_{DD}	0	1	0	0	1	0	1	-	4Ah	4Bh	25h
V_{DD}	V_{DD}	V_{SS}	0	1	0	0	1	1	0	-	4Ch	4Dh	26h
V_{DD}	V_{DD}	V_{DD}	0	1	0	0	1	1	1	-	4Eh	4Fh	27h

Table 5. PCF8574A address map

Pin connectivity			Address of PCF8574A								Address byte value		7-bit hexadecimal address without R/W
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	R/W	Write	Read	
V_{SS}	V_{SS}	V_{SS}	0	1	1	1	0	0	0	-	70h	71h	38h
V_{SS}	V_{SS}	V_{DD}	0	1	1	1	0	0	1	-	72h	73h	39h
V_{SS}	V_{DD}	V_{SS}	0	1	1	1	0	1	0	-	74h	75h	3Ah
V_{SS}	V_{DD}	V_{DD}	0	1	1	1	0	1	1	-	76h	77h	3Bh
V_{DD}	V_{SS}	V_{SS}	0	1	1	1	1	0	0	-	78h	79h	3Ch
V_{DD}	V_{SS}	V_{DD}	0	1	1	1	1	0	1	-	7Ah	7Bh	3Dh
V_{DD}	V_{DD}	V_{SS}	0	1	1	1	1	1	0	-	7Ch	7Dh	3Eh
V_{DD}	V_{DD}	V_{DD}	0	1	1	1	1	1	1	-	7Eh	7Fh	3Fh

8. I/O programming

8.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power on, all the ports are HIGH with a weak 100 μA internal pull-up to V_{DD}, but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the p-channel (transistor to V_{DD}) is small, which saves die size and therefore cost. LED drive only requires an internal transistor to ground, while the LED is connected to V_{DD} through a current-limiting resistor. Totem pole I/O have both n-channel and p-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor — good for logic levels.
- Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.
- Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

Input HIGH: The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to V_{DD} or drives logic 1, then the master will read the value of 1.

Input LOW: The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to V_{SS} or drives logic 0, which sinks the weak 100 μA current source, then the master will read the value of 0.

Output HIGH: The master writes 1 to the register. There is an additional 'accelerator' or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port's 100 μA current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to V_{SS}/driving the port with logic 0 at the same time. After the half clock cycle there is only the 100 μA current source to hold the port HIGH.

Output LOW: The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

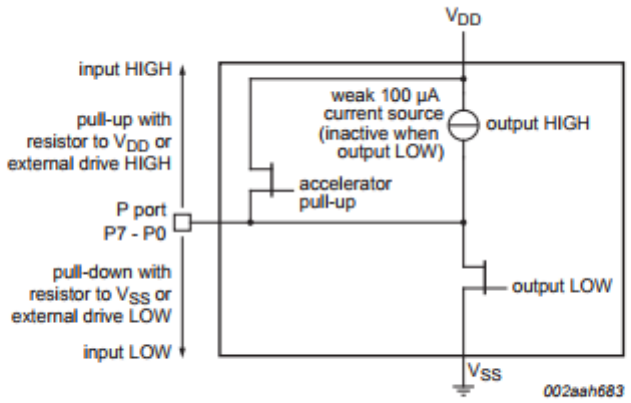


Fig 7. Simple quasi-bidirectional I/O

8.2 Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PCF8574/74A acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PCF8574/74A. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for ½ of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged.

Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.

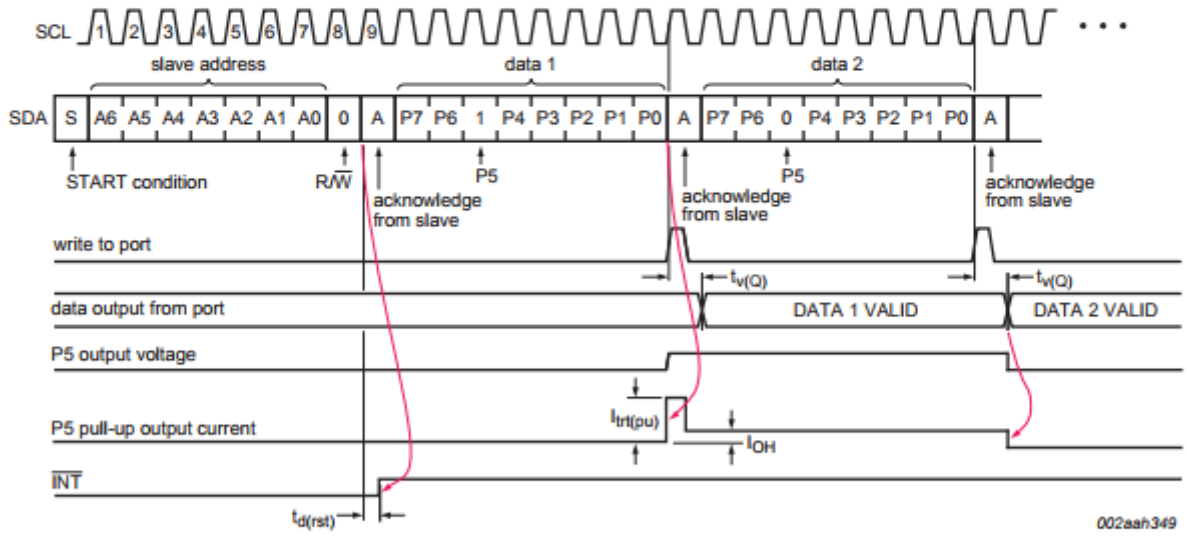


Fig 8. Write mode (output)

Simple code WRITE mode:

<S> <slave address + write> <**ACK**> <data out> <**ACK**> <data out> <**ACK**> ... <data out> <**ACK**> <P>

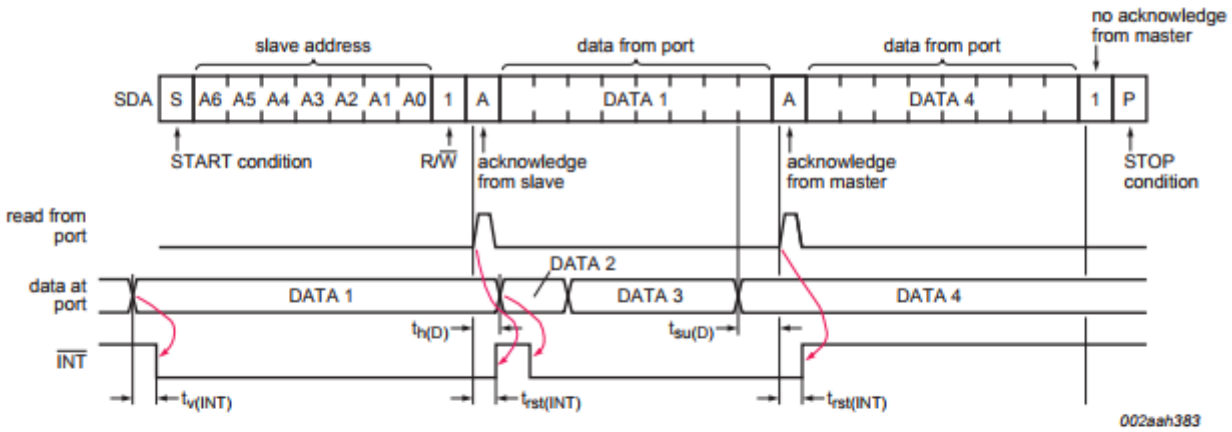
Remark: Bold type = generated by slave device.

8.3 Reading from a port (Input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset. To enter the Read mode the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the pin.

If the data on the input port changes faster than the master can read, this data may be lost. The DATA 2 and DATA3 are lost because these data did not meet the setup time and hold time (see Figure 9).



A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig 9. Read mode (input)

Simple code for Read mode:

<S> <slave address + read> **<ACK>** **<data in>** <ACK> ... **<data in>** <ACK> **<data in>** <NACK> <P>

Remark: Bold type = generated by slave device.

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCF8574/74A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCF8574/74A registers and I^2C-bus/SMBus state machine will initialize to their default states of all I/Os to inputs with weak current source to V_{DD}. Thereafter V_{DD} must be lowered below V_{POR} and back up to the operation voltage for power-on reset cycle.

8.5 Interrupt output ($\overline{INT}$)

The PCF8574/74A provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figure 10). As soon as a port input is changed, the $\overline{INT}$ will be active (LOW) and notify the microcontroller.

An interrupt is generated at any rising or falling edge of the port inputs. After time $t_{v(Q)}$, the signal $\overline{INT}$ is valid.

The interrupt will reset to HIGH when data on the port is changed to the original setting or data is read or written by the master.

In the Write mode, the interrupt may be reset (HIGH) on the rising edge of the acknowledge bit of the address byte and also on the rising edge of the write to port pulse. The interrupt will always be reset (HIGH) on the falling edge of the write to port pulse (see Figure 8).

The interrupt is reset (HIGH) in the Read mode on the rising edge of the read from port pulse (see Figure 9).

During the interrupt reset, any I/O change close to the read or write pulse may not generate an interrupt, or the interrupt will have a very short pulse. After the interrupt is reset, any change in I/Os will be detected and transmitted as an $\overline{INT}$.

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

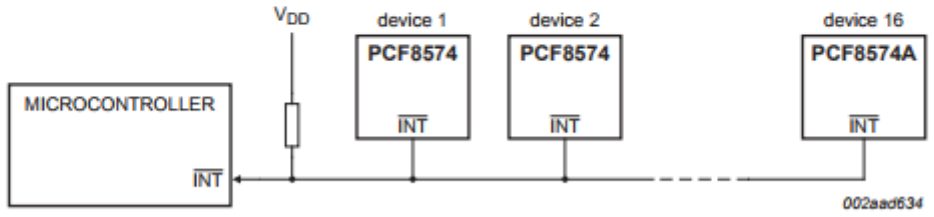


Fig 10. Application of multiple PCF8574/74As with interrupt

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-wire communication between different ICs or modules. The two wires are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 11).

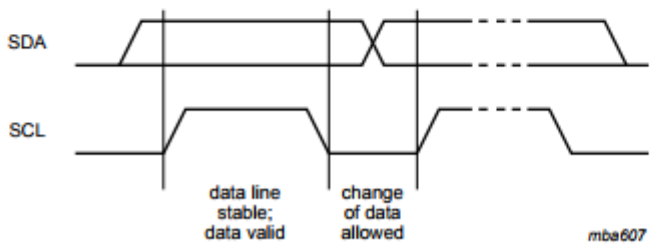


Fig 11. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 12).

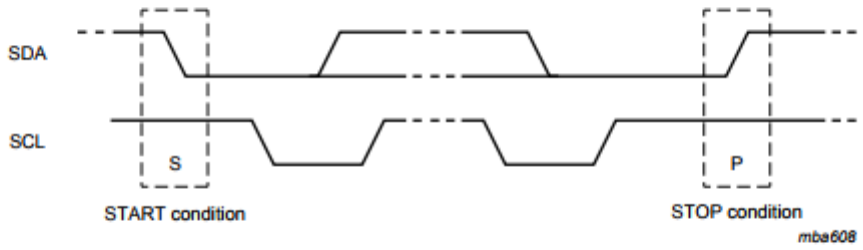


Fig 12. Definition of START and STOP conditions

9.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 13).

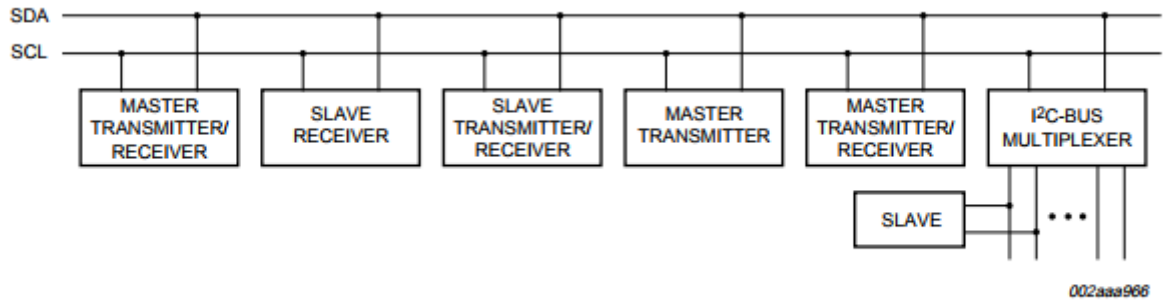


Fig 13. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Figure 14). The acknowledge bit is an active LOW level (generated by the receiving device) that indicates to the transmitter that the data transfer was successful.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that wants to issue an acknowledge bit has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge bit related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

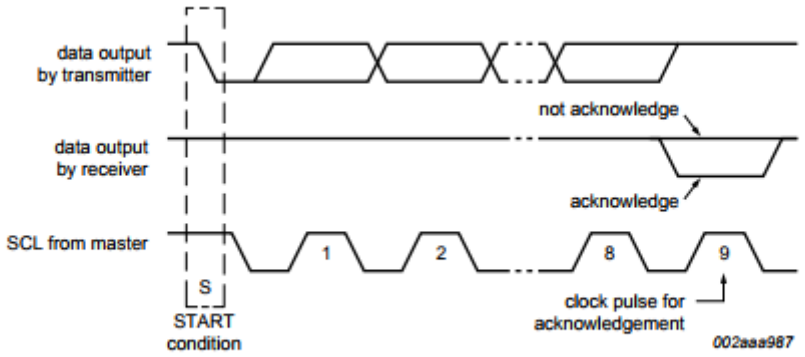


Fig 14. Acknowledgement on the I²C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 15, P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, **the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports**. The desired HIGH or LOW logic levels may be written to the ports used as outputs (P2 to P7). If 10 μA internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line ($\overline{INT}$) that can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there has been a change of data on its ports without having to communicate via the I²C-bus.

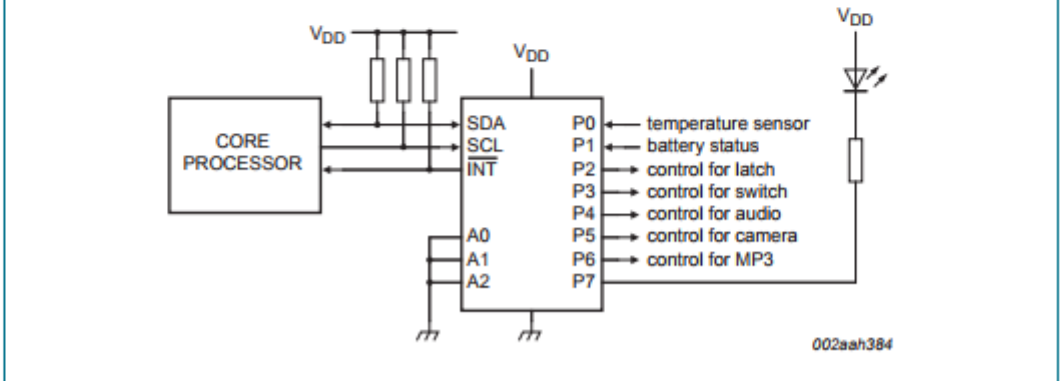


Fig 15. Bidirectional I/O expander application

10.2 How to read and write to I/O expander (example)

In the application example of PCF8574 shown in Figure 15, the microcontroller wants to control the P3 switch ON and the P7 LED ON when the temperature sensor P0 changes.

1. When the system power on:

   Core Processor needs to issue an initial command to set P0 and P1 as inputs and P[7:2] as outputs with value 1010 00 (LED off, MP3 off, camera on, audio off, switch off and latch off).

2. Operation:

   When the temperature changes above the threshold, the temperature sensor signal will toggle from HIGH to LOW. The $\overline{INT}$ will be activated and notifies the 'core processor' that there have been changes on the input pins. Read the input register. If P0 = 0 (temperature sensor has changed), then turn on LED and turn on switch.

3. Software code:

```
//System Power on
// write to PCF8574 with data 1010 0011b to set P[7:2] outputs and P[1:0] inputs
<S> <0100 0000> <ACK> <1010 0011> <ACK> <P>//Initial setting for PCF9574
```

10.3 High current-drive load applications

The GPIO has a minimum guaranteed sinking current of 10 mA per bit at 5 V. In applications requiring additional drive, two port pins may be connected together to sink up to 20 mA current. Both bits must then always be turned on or off together. Up to five pins can be connected together to drive 80 mA, which is the device recommended total limit. Each pin needs its own limiting resistor as shown in Figure 16 to prevent damage to the device should all ports not be turned on at the same time.

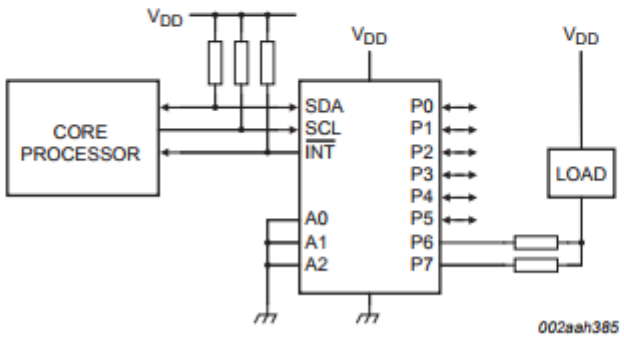


Fig 16. High current-drive load application

10.4 Migration path

NXP offers newer, more capable drop-in replacements for the PCF8574/74A in newer space-saving packages.

Table 6. Migration path

Type number	I²C-bus frequency	Voltage range	Number of addresses per device	Interrupt	Reset	Total package sink current
PCF8574/74A	100 kHz	2.5 V to 6 V	8	yes	no	80 mA
PCA8574/74A	400 kHz	2.3 V to 5.5 V	8	yes	no	200 mA
PCA9674/74A	1 MHz Fm+	2.3 V to 5.5 V	64	yes	no	200 mA
PCA9670	1 MHz Fm+	2.3 V to 5.5 V	64	no	yes	200 mA
PCA9672	1 MHz Fm+	2.3 V to 5.5 V	16	yes	yes	200 mA

PCA9670 replaces the interrupt output of the PCA9674 with hardware reset input to retain the maximum number of addresses and the PCA9672 replaces address A2 of the PCA9674 with hardware reset input to retain the interrupt but limit the number of addresses.

11. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+7	V
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
V_I	input voltage		V_{SS} – 0.5	V_{DD} + 0.5	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
$T_{j(max)}$	maximum junction temperature		-	125	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO16 package	115	°C/W
		SSOP20 package	136	°C/W

13. Static characteristics

Table 9. Static characteristics

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.5	-	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz		-	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}		-	2.5	10	µA
V_{POR}	power-on reset voltage	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}	[1]	-	1.3	2.4	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			–0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	V_{DD} + 0.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		–1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	-	7	pF
I/Os; P0 to P7							
V_{IL}	LOW-level input voltage			–0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	V_{DD} + 0.5	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$		-	-	±400	µA
I_{OL}	LOW-level output current	V_{OL} = 1 V; V_{DD} = 5 V		10	25	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$		30	-	300	µA
$I_{trt(pu)}$	transient boosted pull-up current	HIGH during acknowledge (see Figure 8); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V		-	–1	-	mA

C_i	input capacitance		-	-	10	pF
C_o	output capacitance		-	-	10	pF
Interrupt $\overline{INT}$ (see Figure 8)						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
Select inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	−250	-	+250	nA

[1] The power-on reset circuit resets the I^2C-bus logic at $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

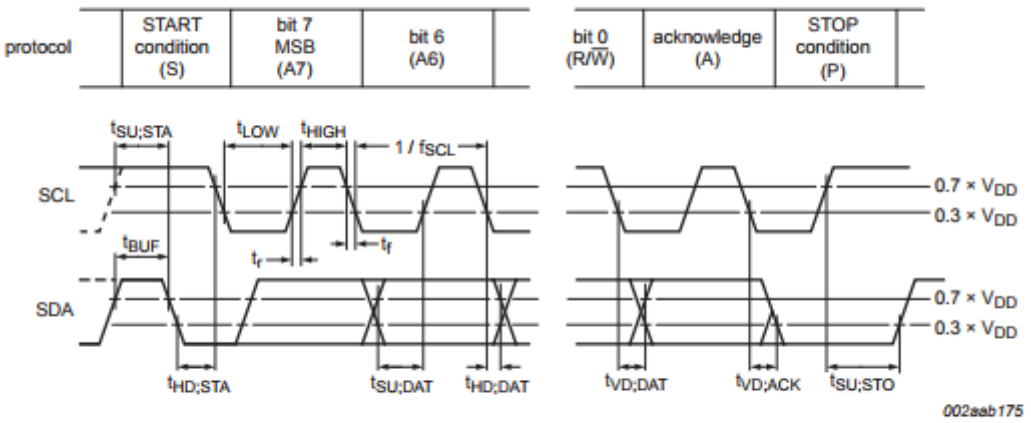
14. Dynamic characteristics

Table 10. Dynamic characteristics

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I^2C-bus timing[1] (see Figure 17)						
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{VD;DAT}$	data valid time		-	-	3.4	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		4	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
Port timing (see Figure 8 and Figure 9)						
$t_{v(Q)}$	data output valid time	$C_L \leq 100$ pF	-	-	4	µs
$t_{su(D)}$	data input set-up time	$C_L \leq 100$ pF	0	-	-	µs
$t_{h(D)}$	data input hold time	$C_L \leq 100$ pF	4	-	-	µs
Interrupt $\overline{INT}$ timing (see Figure 9)						
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from port to $\overline{INT}$; $C_L \leq 100$ pF	-	-	4	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$; $C_L \leq 100$ pF	-	-	4	µs

[1] All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 17. I²C-bus timing diagram