ANALOG DEVICES

14-Bit, 210 MSPS TxDAC® D/A Converter
AD9744

FEATURES

High performance member of pin-compatible
  TxDAC product family
Excellent spurious-free dynamic range performance
SFDR to Nyquist
    83 dBc at 5 MHz output
    80 dBc at 10 MHz output
    73 dBc at 20 MHz output
SNR at 5 MHz output, 125 MSPS: 77 dB
Twos complement or straight binary data format
Differential current outputs: 2 mA to 20 mA
Power dissipation: 135 mW at 3.3 V
Power-down mode: 15 mW at 3.3 V
On-chip 1.2 V reference
CMOS-compatible digital interface
28-lead SOIC, 28-lead TSSOP, and 32-lead LFCSP packages
Edge-triggered latches

APPLICATIONS

Wideband communication transmit channel
    Direct IFs
    Base stations
    Wireless local loops
    Digital radio links
    Direct digital synthesis (DDS)
    Instrumentation

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD9744[1] is a 14-bit resolution, wideband, third generation member of the TxDAC series of high performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, consisting of pin-compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD9744 offers exceptional ac and dc performance while supporting update rates up to 210 MSPS.

The AD9744's low power dissipation makes it well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 60 mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 15 mW. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance.
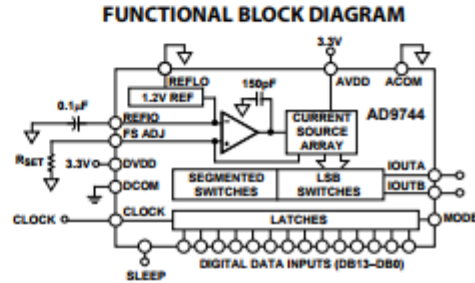
Edge-triggered input latches and a 1.2 V temperature compensated band gap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support 3 V CMOS logic families.

PRODUCT HIGHLIGHTS

1. The AD9744 is the 14-bit member of the pin compatible TxDAC family, which offers excellent INL and DNL performance.
2. Data input supports twos complement or straight binary data coding.
3. High speed, single-ended CMOS clock input supports 210 MSPS conversion rate.
4. Low power: Complete CMOS DAC function operates on 135 mW from a 2.7 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.
5. On-chip voltage reference: The AD9744 includes a 1.2 V temperature compensated band gap voltage reference.
6. Industry-standard 28-lead SOIC, 28-lead TSSOP, and 32-lead LFCSP packages.

[1]Protected by U.S. Patent Numbers 5568145, 5689257, and 5703519.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	−5	±0.8	+5	LSB
Differential Nonlinearity (DNL)	−3	±0.5	+3	LSB
ANALOG OUTPUT				
Offset Error	−0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	−0.5	±0.1	+0.5	% of FSR
Gain Error (With Internal Reference)	−0.5	±0.1	+0.5	% of FSR
Full-Scale Output Current[2]	2		20	mA
Output Compliance Range	−1		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (External Reference)		7		kΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	2.7	3.3	3.6	V
DVDD	2.7	3.3	3.6	V
CLKVDD	2.7	3.3	3.6	V
Analog Supply Current (I_{AVDD})		33	36	mA
Digital Supply Current (I_{DVDD})[4]		8	9	mA
Clock Supply Current (I_{CLKVDD})		5	6	mA
Supply Current Sleep Mode (I_{AVDD})		5	6	mA
Power Dissipation[4]		135	145	mW
Power Dissipation[5]		145		mW
Power Supply Rejection Ratio—AVDD[6]	−1		+1	% of FSR/V
Power Supply Rejection Ratio—DVDD[6]	−0.04		+0.04	% of FSR/V
OPERATING RANGE	−40		+85	°C

[1] Measured at IOUTA, driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[3] An external buffer amplifier with input bias current <100 nA should be used to drive any external load.
[4] Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1 MHz.
[5] Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.
[6] ±5% power supply variation.

DYNAMIC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, differential transformer coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	210			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)[2]		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)[2]		30		pA/√Hz
Noise Spectral Density[3]		−155		dBm/Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	77	90		dBc
−6 dBFS Output		87		dBc
−12 dBFS Output		82		dBc
−18 dBFS Output		82		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 1.00 MHz		85		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.51 MHz		84		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10 MHz		80		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15 MHz		75		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 25 MHz		74		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 21 MHz		73		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 41 MHz		60		dBc
f_{CLOCK} = 210 MSPS; f_{OUT} = 41 MHz		68		dBc
f_{CLOCK} = 210 MSPS; f_{OUT} = 69 MHz		64		dBc
Spurious-Free Dynamic Range Within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz; 2 MHz Span	84	90		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		90		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.03 MHz; 2.5 MHz Span		87		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		87		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		−86	−77	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.00 MHz		−77		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz		−77		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 2.00 MHz		−77		dBc
Signal-to-Noise Ratio				
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		82		dB
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		88		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		77		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		78		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		70		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		70		dB
f_{CLOCK} = 210 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		74		dB
f_{CLOCK} = 210 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		67		dB

Parameter	Min	Typ	Max	Unit
Multitone Power Ratio (8 Tones at 400 kHz Spacing)				
f_{CLOCK} = 78 MSPS; f_{OUT} = 15.0 MHz to 18.2 MHz				
0 dBFS Output		66		dBc
−6 dBFS Output		68		dBc
−12 dBFS Output		62		dBc
−18 dBFS Output		61		dBc

[1] Measured single-ended into 50 Ω load.
[2] Output noise is measured with a full-scale output set to 20 mA with no conversion activity. It is a measure of the thermal noise only.
[3] Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS[1]				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current	−10		+10	μA
Logic 0 Current	−10		+10	μA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulse Width (t_{LPW})	1.5			ns
CLK INPUTS[2]				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V

[1] Includes CLOCK pin on SOIC/TSSOP packages and CLK+ pin on LFCSP package in single-ended clock input mode.
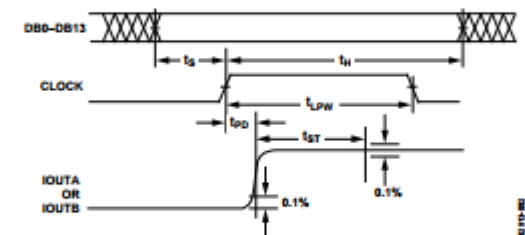[2] Applicable to CLK+ and CLK− inputs when configured for differential or PECL clock input mode.

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect to	Min	Max	Unit
AVDD	ACOM	−0.3	+3.9	V
DVDD	DCOM	−0.3	+3.9	V
CLKVDD	CLKCOM	−0.3	+3.9	V
ACOM	DCOM	−0.3	+0.3	V
ACOM	CLKCOM	−0.3	+0.3	V
DCOM	CLKCOM	−0.3	+0.3	V
AVDD	DVDD	−3.9	+3.9	V
AVDD	CLKVDD	−3.9	+3.9	V
DVDD	CLKVDD	−3.9	+3.9	V
CLOCK, SLEEP	DCOM	−0.3	DVDD + 0.3	V
Digital Inputs, MODE	DCOM	−0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	−1.0	AVDD + 0.3	V
REFIO, REFLO, FS ADJ	ACOM	−0.3	AVDD + 0.3	V
CLK+, CLK−, CMODE	CLKCOM	−0.3	CLKVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
28-Lead 300-Mil SOIC	55.9	°C/W
28-Lead TSSOP	67.7	°C/W
32-Lead LFCSP	32.5	°C/W

ESD CAUTION

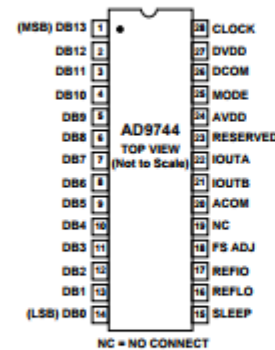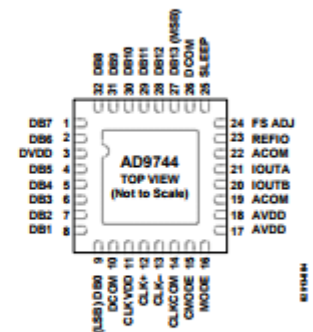# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 3. 28-Lead SOIC and TSSOP

NOTES
1. CONNECT THE EXPOSED PAD THERMALLY TO A COPPER GROUND PLANE FOR ENHANCED ELECTRICAL AND THERMAL PERFORMANCE.

Figure 4. 32-Lead LFCSP

Table 6. Pin Function Descriptions

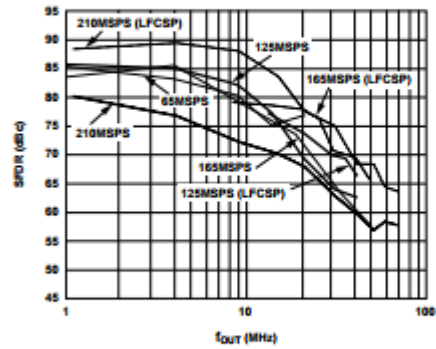| SOIC/TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	27	DB13	Most Significant Data Bit (MSB).
2 to 13	28 to 32, 1, 2, 4 to 8	DB12 to DB1	Data Bits 12 to 1.
14	9	DB0	Least Significant Data Bit (LSB).
15	25	SLEEP	Power-Down Control Input. Active high. Contains active pull-down circuit; it may be left unterminated if not used.
16	N/A	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to ACOM for both internal and external reference operation modes.
17	23	REFIO	Reference Input/Output. Serves as reference input when using external reference. Serves as 1.2 V reference output when using internal reference. Requires 0.1 µF capacitor to ACOM when using internal reference.
18	24	FS ADJ	Full-Scale Current Output Adjust.
19	N/A	NC	No Internal Connection.
20	19, 22	ACOM	Analog Common.
21	20	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	21	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	N/A	RESERVED	Reserved. Do not connect to common or supply.
24	17, 18	AVDD	Analog Supply Voltage (3.3 V).
25	16	MODE	Selects Input Data Format. Connect to DCOM for straight binary, DVDD for twos complement.
N/A	15	CMODE	Clock Mode Selection. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK−). Connect to CLKVDD for differential receiver. Float for PECL receiver (terminations on-chip).
26	10, 26	DCOM	Digital Common.
27	3	DVDD	Digital Supply Voltage (3.3 V).
28	N/A	CLOCK	Clock Input. Data latched on positive edge of clock.
N/A	12	CLK+	Differential Clock Input.
N/A	13	CLK−	Differential Clock Input.
N/A	11	CLKVDD	Clock Supply Voltage (3.3 V).
N/A	14	CLKCOM	Clock Common.
N/A	EPAD	EPAD	Exposed Pad. Connect the exposed pad thermally to a copper ground plane for enhanced electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS
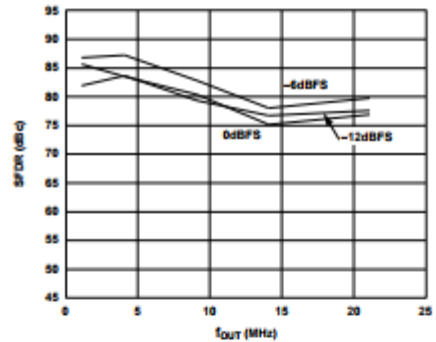

Figure 5. SFDR vs. f_OUT at 0 dBFS
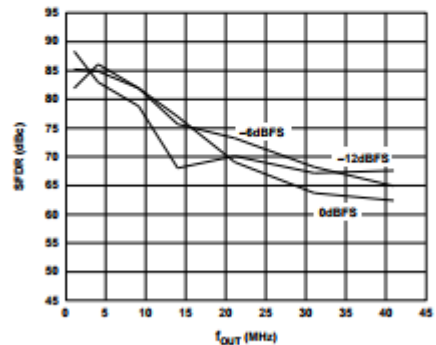

Figure 6. SFDR vs. f_OUT at 65 MSPS

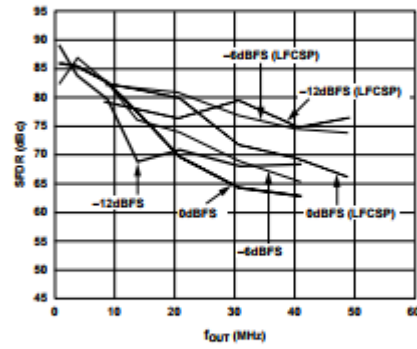*Figure 7. SFDR vs. f_OUT at 125 MSPS*
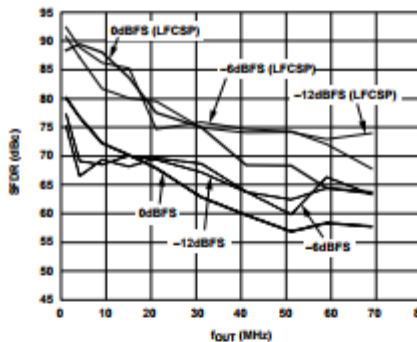

Figure 8. SFDR vs. f_OUT at 165 MSPS

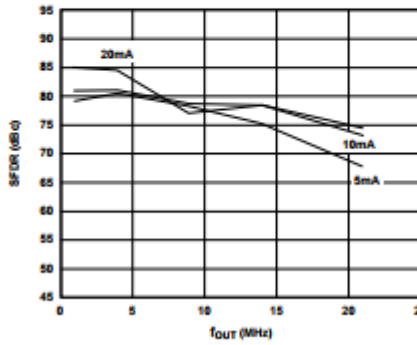*Figure 9. SFDR vs. f_OUT at 210 MSPS*

Figure 10. SFDR vs. f_OUT and I_OUTFS at 65 MSPS and 0 dBFS

EVALUATION BOARD

GENERAL DESCRIPTION

The TxDAC family evaluation boards allow for easy setup and testing of any TxDAC product in the SOIC and LFCSP packages. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to evaluate the AD9744 easily and effectively in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9744 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9744 with either the internal or external reference or to exercise the power-down feature.
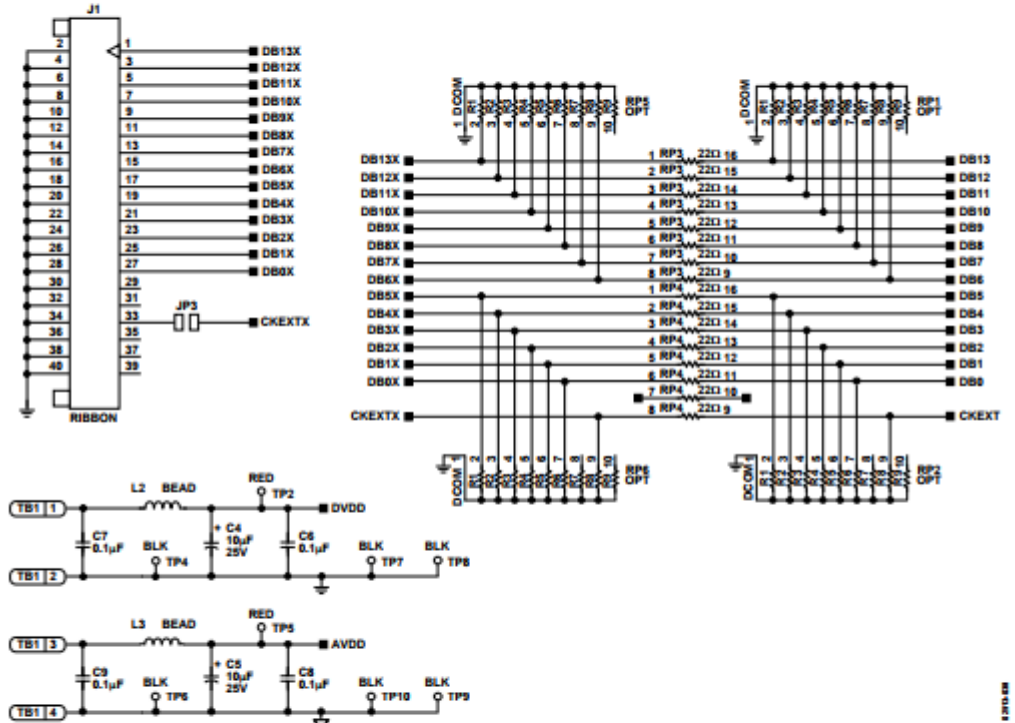

Figure 41. SOIC Evaluation Board—Power Supply and Digital Inputs