High Speed, Video Difference Amplifier

AD830

FEATURES

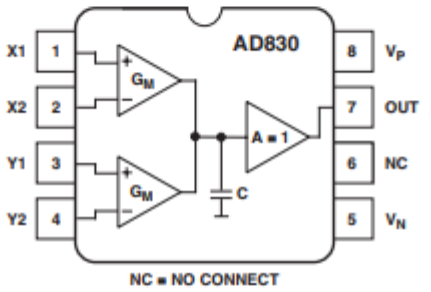
Differential Amplification
Wide Common-Mode Voltage Range: +12.8 V, –12 V
Differential Voltage Range: ±2 V
High CMRR: 60 dB @ 4 MHz
Built-In Differential Clipping Level: ±2.3 V
Fast Dynamic Performance
85 MHz Unity Gain Bandwidth
35 ns Settling Time to 0.1%
360 V/μs Slew Rate
Symmetrical Dynamic Response
Excellent Video Specifications
Differential Gain Error: 0.06%
Differential Phase Error: 0.08°
15 MHz (0.1 dB) Bandwidth
Flexible Operation
High Output Drive of ±50 mA Min
Specified with Both ±5 V and ±15 V Supplies
Low Distortion: THD = –72 dB @ 4 MHz
Excellent DC Performance: 3 mV Max Input Offset Voltage

APPLICATIONS

Differential Line Receiver
High Speed Level Shifter
High Speed In-Amp
Differential to Single-Ended Conversion
Resistorless Summation and Subtraction
High Speed A/D Driver

CONNECTION DIAGRAM

8-Lead Plastic PDIP (N), CERDIP (Q) and SOIC (RN) Packages



NC = NO CONNECT

GENERAL DESCRIPTION

The AD830 is a wideband, differencing amplifier designed for use at video frequencies but also useful in many other applications. It accurately amplifies a fully differential signal at the input and produces an output voltage referred to a user-chosen level. The undesired common-mode signal is rejected, even at high frequencies. High impedance inputs ease interfacing to finite source impedances and thus preserve the excellent common-mode rejection. In many respects, it offers significant improvements over discrete difference amplifier approaches, in particular in high frequency common-mode rejection.

The wide common-mode and differential voltage range of the AD830 make it particularly useful and flexible in level shifting applications, but at lower power dissipation than discrete solutions. Low distortion is preserved over the many possible differential and common-mode voltages at the input and output.

Good gain flatness and excellent differential gain of 0.06% and phase of 0.08° make the AD830 suitable for many video system applications. Furthermore, the AD830 is suited for general-purpose signal processing from dc to 10 MHz.

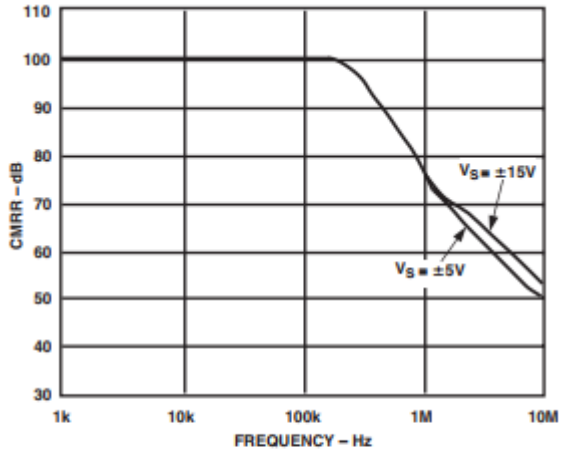


Figure 1. Common-Mode Rejection Ratio vs. Frequency

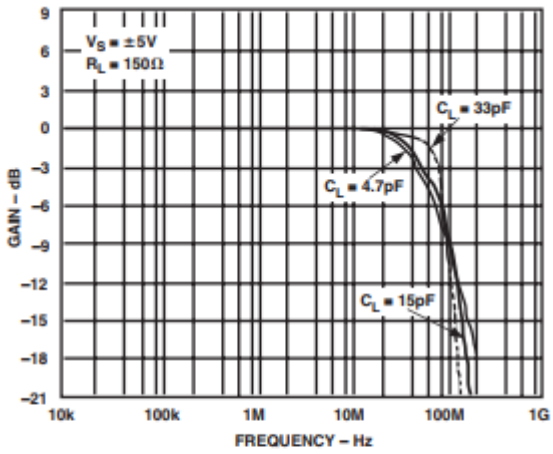


Figure 2. Closed-Loop Gain vs. Frequency, Gain = +1

REV. B

AD830–SPECIFICATIONS (V_S = ±15 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	AD830J/AD830A Min	AD830J/AD830A Typ	AD830J/AD830A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Unit
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = +1, V_{OUT} = 100 mV rms	75	85		75	85		MHz
0.1 dB Gain Flatness Frequency	Gain = +1, V_{OUT} = 100 mV rms	11	15		11	15		MHz
Differential Gain Error	0 V to 0.7 V, Frequency = 4.5 MHz		0.06	0.09		0.06	0.09	%
Differential Phase Error	0 V to 0.7 V, Frequency = 4.5 MHz		0.08	0.12		0.08	0.12	Degrees
Slew Rate	2 V Step, R_L = 500 Ω		360			360		V/µs
	4 V Step, R_L = 500 Ω		350			350		V/µs
3 dB Large Signal Bandwidth	Gain = +1, V_{OUT} = 1 V rms	38	45		38	45		MHz
Settling Time, Gain = +1	V_{OUT} = 2 V Step, to 0.1%		25			25		ns
	V_{OUT} = 4 V Step, to 0.1%		35			35		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–82			–82		dBc
	2 V p-p, Frequency = 4 MHz		–72			–72		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = +1		±1.5	±3		±1.5	±3	mV
	Gain = +1, T_{MIN} – T_{MAX}			±5			±7	mV
Open-Loop Gain	DC	64	69		64	69		dB
Gain Error	R_L = 1 kΩ, G = ±1		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L = 1 kΩ,	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
Gain = +1	–1.5 V ≤ X ≤ +1.5 V		0.035	0.07		0.035	0.07	% FS
	–2 V ≤ X ≤ +2 V		0.15	0.4		0.15	0.4	% FS
Input Bias Current	V_{IN} = 0 V, 25°C to T_{MAX}		5	10		5	10	µA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN} – T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.1	±2.3		±2.1	±2.3		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–12.0		+12.8	–12.0		+12.8	V
CMRR	DC, Pins 1, 2, ±10 V	90	100		90	100		dB
	DC, Pins 1, 2, ±10 V, T_{MIN} – T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 1 kΩ	±12	+13.8, –13.8		±12	+13.8, –13.8		V
	R_L ≥ 1 kΩ, ±16.5 V_S	±13	+15.3, –14.7		±13	+15.3, –14.7		V
Short-Circuit Current	Short to Ground		±80			±80		mA
Output Current	R_L = 150 Ω	±50			±50			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN} – T_{MAX}		14.5	17		14.5	17	mA
+ PSRR (to V_P)	DC, G = +1		86			86		dB
– PSRR (to V_N)	DC, G = +1		68			68		dB
PSRR	DC, G = +1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR	DC, G = +1, ±5 to ±15 V_S, T_{MIN} – T_{MAX}	62	68		60	68		dB

NOTES
[1]See Standard Military Drawing 5962-9313001MPA for specifications.
[2]Clipping level function on X channel only.

Specifications subject to change without notice.

SPECIFICATIONS (V_S = ±5 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C, unless otherwise noted.)

Parameter	Conditions	AD830J/AD830A Min	AD830J/AD830A Typ	AD830J/AD830A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Unit
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = +1, V_{OUT} = 100 mV rms	35	40		35	40		MHz
0.1 dB Gain Flatness Frequency	Gain = +1, V_{OUT} = 100 mV rms	5	6.5		5	6.5		MHz
Differential Gain Error	0 V to 0.7 V, Frequency = 4.5 MHz, Gain = +2		0.14	0.18		0.14	0.18	%
Differential Phase Error	0 V to 0.7 V, Frequency = 4.5 MHz, Gain = +2		0.32	0.4		0.32	0.4	Degrees
Slew Rate, Gain = +1	2 V Step, R_L = 500 Ω		210			210		V/µs
	4 V Step, R_L = 500 Ω		240			240		V/µs
3 dB Large Signal Bandwidth	Gain = +1, V_{OUT} = 1 V rms	30	36		30	36		MHz
Settling Time	V_{OUT} = 2 V Step, to 0.1%		35			35		ns
	V_{OUT} = 4 V Step, to 0.1%		48			48		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–69			–69		dBc
	2 V p-p, Frequency = 4 MHz		–56			–56		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = +1		±1.5	±3		±1.5	±3	mV
	Gain = +1, T_{MIN} – T_{MAX}			±4			±5	mV
Open-Loop Gain	DC	60	65		60	65		dB
Unity Gain Accuracy	R_L = 1 kΩ		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L = 1 kΩ	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
	–1.5 V ≤ X ≤ +1.5 V		0.045	0.07		0.045	0.07	% FS
	–2 V ≤ X ≤ +2 V		0.23	0.4		0.23	0.4	% FS
Input Bias Current	V_{IN} = 0 V, 25°C to T_{MAX}		5	10		5	10	µA
	V_{IN} = 0 V, T_{MIN}		7	13		8	17	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN} – T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level[2]	Pins 1 and 2 Inputs Only	±2.0	±2.2		±2.0	±2.2		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–2.0		+2.9	–2.0		+2.9	V
CMRR	DC, Pins 1, 2, +4 V to –2 V	90	100		90	100		dB
	DC, Pins 1, 2, +4 V to –2 V, T_{MIN} – T_{MAX}	88			86			dB
	Frequency = 4 MHz	55	60		55	60		dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 150 Ω	±3.2	±3.5		±3.2	±3.5		V
	R_L ≥ 150 Ω, ±4 V_S	±2.2	–2.4, +2.7		±2.2	–2.4, +2.7		V
Short-Circuit Current	Short to Ground		–55, +70			–55, +70		mA
Output Current		±40			±40			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN} – T_{MAX}		13.5	16		13.5	16	mA
+ PSRR (to V_P)	DC, G = +1, Offset		86			86		dB
– PSRR (to V_N)	DC, G = +1, Offset		68			68		dB
PSRR (Dual-Supply)	DC, G = +1, ±5 to ±15 V_S	66	71		66	71		dB
PSRR (Dual-Supply)	DC, G = +1, ±5 to ±15 V_S, T_{MIN} – T_{MAX}	62	68		60	68		dB

NOTES

[1]See Standard Military Drawing 5962-9313001MPA for specifications.

[2]Clipping level function on X channel only.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	Observe Derating Curves
Output Short-Circuit Duration	Observe Derating Curves
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range (Q)	–65°C to +150°C
Storage Temperature Range (N)	–65°C to +125°C
Storage Temperature Range (RN)	–65°C to +125°C
Operating Temperature Range	
AD830J	0°C to +70°C
AD830A	–40°C to +85°C
AD830S	–55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Lead PDIP Package: θ_{JA} = 90°C/W.
8-Lead SOIC Package: θ_{JA} = 155°C/W.
8-Lead CERDIP Package: θ_{JA} = 110°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD830 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the CERDIP, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the AD830 in the overheated condition for an extended period can result in permanent damage to the device. To ensure proper operation, it is important to observe the recommended derating curves.

While the AD830 output is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. If the output is shorted to a supply rail for an extended period, then the amplifier may be permanently destroyed.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD830AN	–40°C to +85°C	8-Lead PDIP	N-8
AD830JR	0°C to +70°C	8-Lead SOIC	RN-8
5962-9313001MPA*	–55°C to +125°C	8-Lead CERDIP	Q-8
AD830AR	–40°C to +85°C	8-Lead SOIC	RN-8
AD830AR-REEL	–40°C to +85°C	8-Lead SOIC	RN-8
AD830AR-REEL7	–40°C to +85°C	8-Lead SOIC	RN-8
AD830JR-REEL	0°C to 70°C	8-Lead SOIC	RN-8
AD830JR-REEL7	0°C to 70°C	8-Lead SOIC	RN-8

*See Standard Military Drawing 5962-9313001 MPA for specifications.

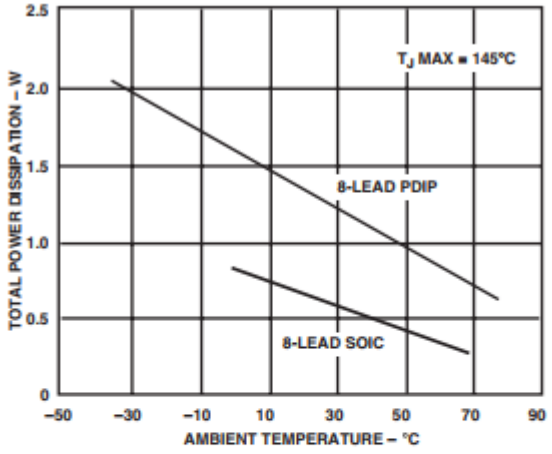


Figure 3. Maximum Power Dissipation vs. Temperature, PDIP and SOIC Packages

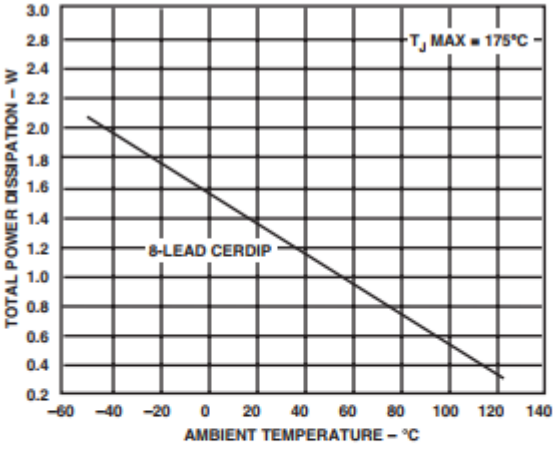
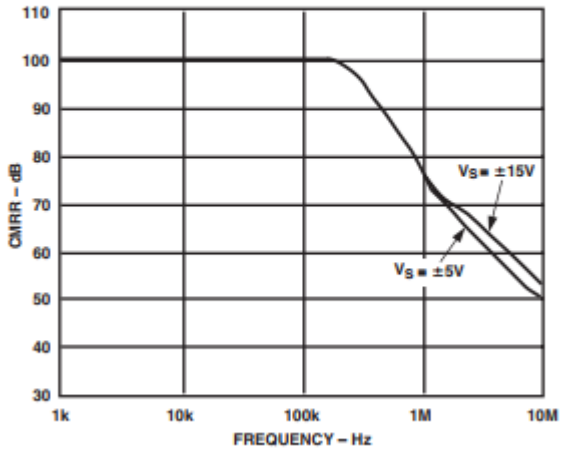


Figure 4. Maximum Power Dissipation vs. Temperature, CERDIP Package

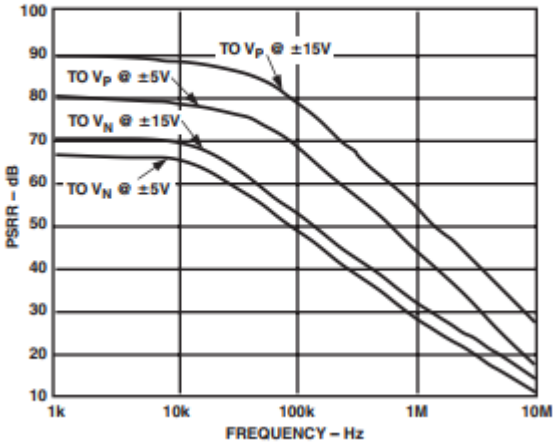
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD830 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

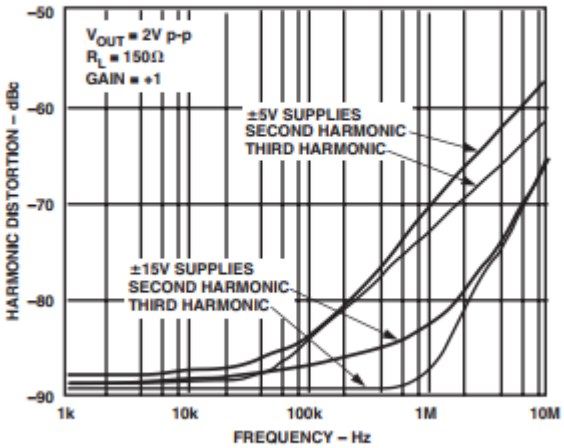
Typical Performance Characteristics–AD830



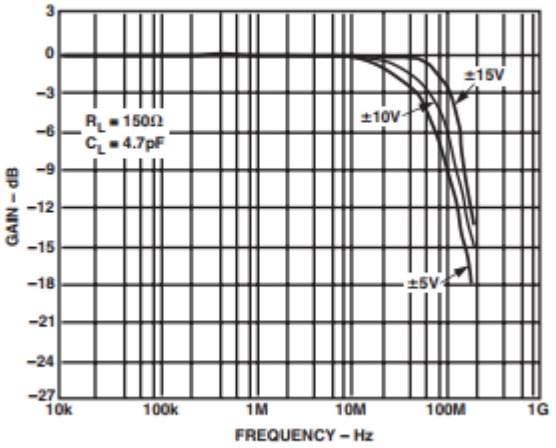
TPC 1. Common-Mode Rejection Ratio vs. Frequency



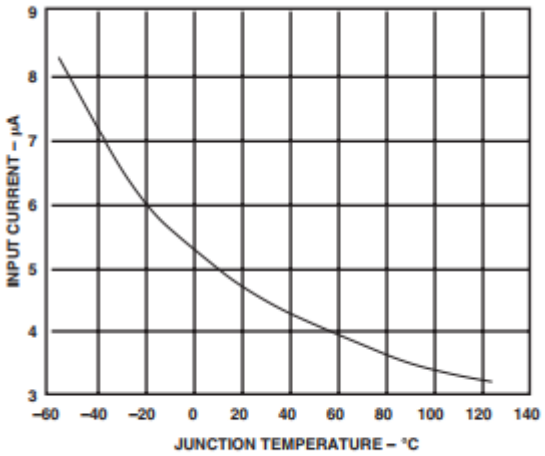
TPC 4. Power Supply Rejection Ratio vs. Frequency



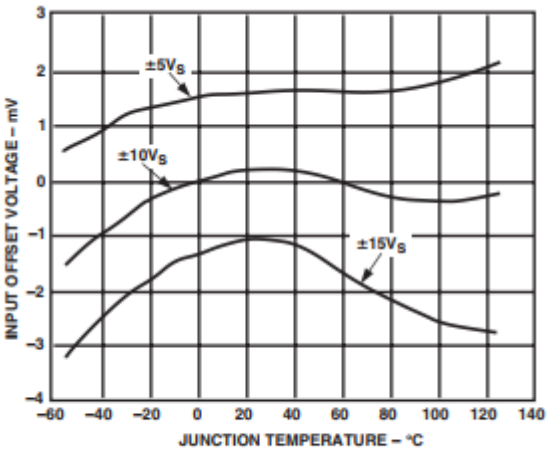
TPC 2. Harmonic Distortion vs. Frequency



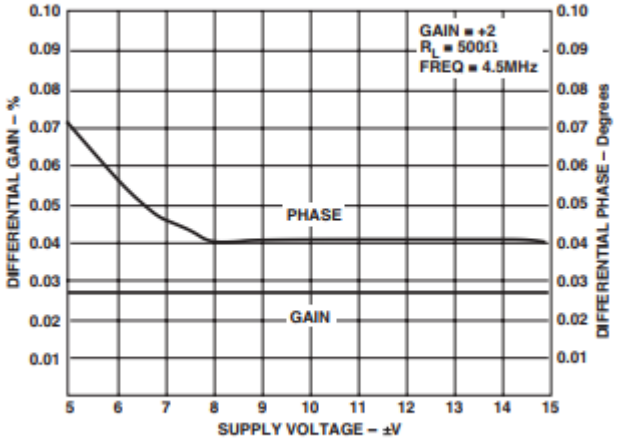
TPC 5. Closed-Loop Gain vs. Frequency G = +1



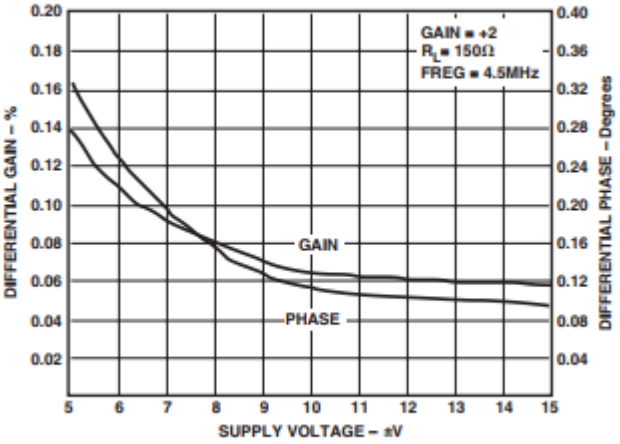
TPC 3. Input Bias Current vs. Temperature



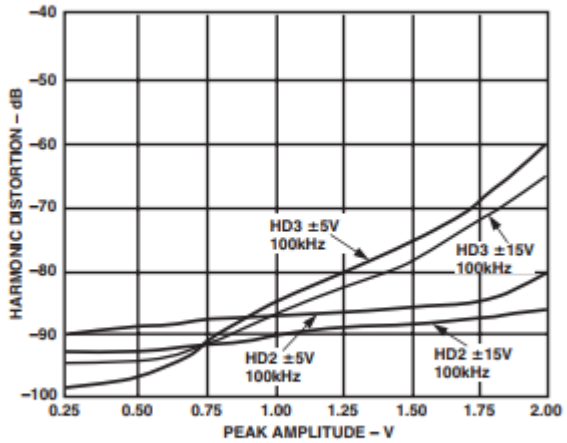
TPC 6. Input Offset Voltage vs. Temperature



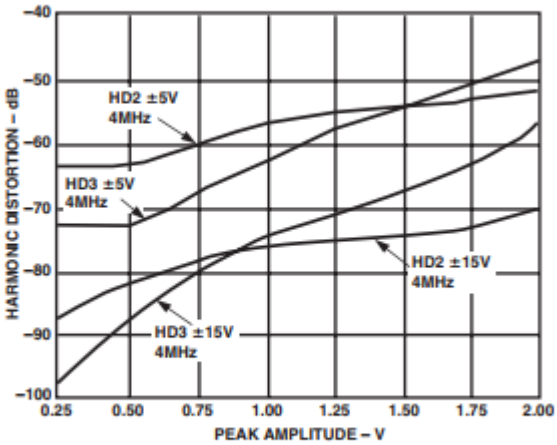
TPC 7. Differential Gain and Phase vs. Supply Voltage, R_L = 500 Ω



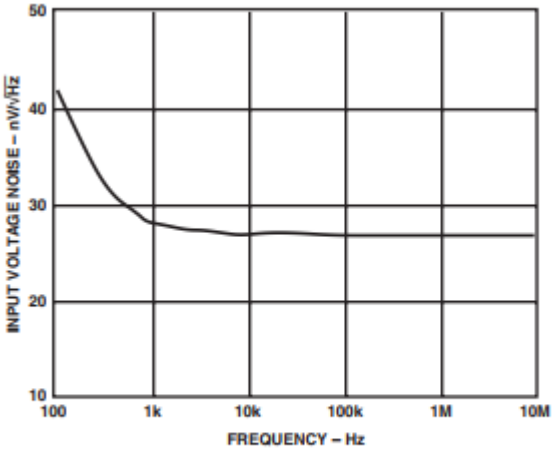
TPC 10. Differential Gain and Phase vs. Supply Voltage, R_L = 150 Ω



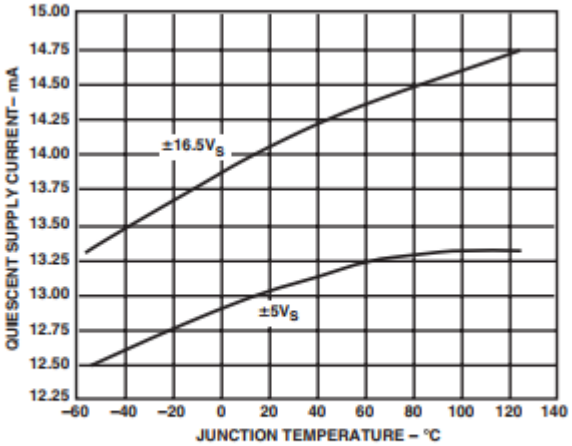
TPC 8. Harmonic Distortion vs. Peak Amplitude, Frequency = 100 kHz



TPC 11. Harmonic Distortion vs. Peak Amplitude, Frequency = 4 MHz



TPC 9. Noise Spectral Density



TPC 12. Supply Current vs. Junction Temperature

TRADITIONAL DIFFERENTIAL AMPLIFICATION

In the past, when differential amplification was needed to reject common-mode signals superimposed with a desired signal, most often the solution used was the classic op amp based difference amplifier shown in Figure 5. The basic function $V_O = V_1 - V_2$ is simply achieved, but the overall performance is poor and the circuit possesses many serious problems that make it difficult to realize a robust design with moderate to high levels of performance.

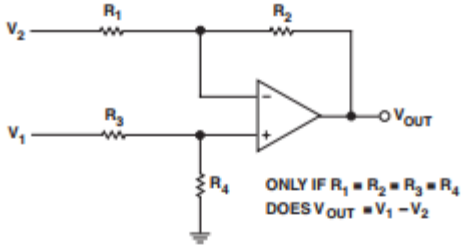


Figure 5. Op Amp Based Difference Amplifier

PROBLEMS WITH THE OP AMP BASED APPROACH

- Low common-mode rejection ratio (CMRR)
- Low impedance inputs
- CMRR highly sensitive to the value of source R
- Different input impedance for the + and – input
- Poor high frequency CMRR
- Requires very highly matched resistors $R_1 - R_4$ to achieve high CMRR
- Halves the bandwidth of the op amp
- High power dissipation in the resistors for large common-mode voltage

AD830 FOR DIFFERENTIAL AMPLIFICATION

The AD830 amplifier was specifically developed to solve the listed problems with the discrete difference amplifier approach. Its topology, discussed in detail in the Understanding the AD830 Topology section, by design acts as a difference amplifier. The circuit of Figure 6 shows how simply the AD830 is configured to produce the difference of the two signals, V_1 and V_2, in which the applied differential signal is exactly reproduced at the output relative to a separate output common. Any common-mode voltage present at the input is removed by the AD830.

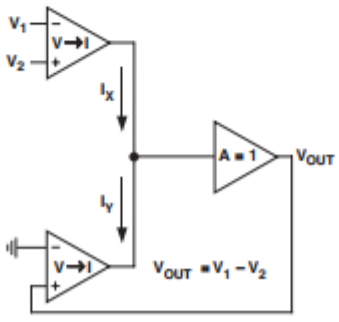


Figure 6. AD830 as a Difference Amplifier

ADVANTAGEOUS PROPERTIES OF THE AD830

- High common-mode rejection ratio (CMRR)
- High impedance inputs
- Symmetrical dynamic response for +1 and –1 Gain
- Low sensitivity to the value of source R
- Equal input impedance for the + and – input
- Excellent high frequency CMRR
- No halving of the bandwidth
- Constant power distortion versus common-mode voltage
- Highly matched resistors not needed

UNDERSTANDING THE AD830 TOPOLOGY

The AD830 represents Analog Devices' first amplifier product to embody a powerful alternative amplifier topology. Referred to as active feedback, the topology used in the AD830 provides inherent advantages in the handling of differential signals, differing system commons, level shifting, and low distortion, high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits or superior to op amp based equivalent circuits. With this in mind, it is important to understand the internal structure of the AD830.

The topology, reduced to its elemental form, is shown in Figure 7. Nonideal effects, such as nonlinearity, bias currents, and limited full scale, are omitted from this model for simplicity, but are discussed later. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage-to-current converters possess fully differential inputs, high linearity, high input impedance, and wide voltage range operation. This enables the part to handle large amplitude differential signals; it also provides high common-mode rejection, low distortion, and negligible loading on the source. The label G_M is meant to convey that the transconductance is a large signal quantity, unlike in the front end of most op amps. The two G_M stage current outputs, I_X and I_Y, sum together at a high impedance node—which is characterized by an equivalent resistance and capacitance connected to an "ac common." A unity voltage gain stage follows the high impedance node to provide buffering from loads. Relative to either input, the open-loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P; $A_{OL} = G_M \times R_P$. The unity gain frequency $\omega_{0\,dB}$ for the open-loop gain is established by the transconductance, G_M, working into the capacitance, C_C; $\omega_{0\,dB} = G_M/C_C$. The open-loop description of the AD830 is shown below for completeness.

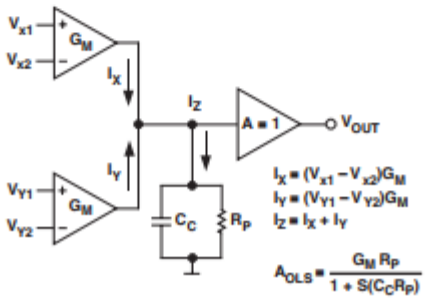


Figure 7. Topology Diagram