ANALOG DEVICES

CMOS 200 MSPS 14-Bit Quadrature Digital Upconverter

AD9857

FEATURES

- 200 MHz internal clock rate
- 14-bit data path
- Excellent dynamic performance:
  - 80 dB SFDR @ 65 MHz (±100 kHz) A_{OUT}
- 4× to 20× programmable reference clock multiplier
- Reference clock multiplier PLL lock detect indicator
- Internal 32-bit quadrature DDS
- FSK capability
- 8-bit output amplitude control
- Single-pin power-down function
- Four programmable, pin-selectable signal profiles
- SIN(x)/x correction (inverse SINC function)
- Simplified control interface
  - 10 MHz serial, 2-wire or 3-wire SPI*-compatible
- 3.3 V single supply
- Single-ended or differential input reference clock
- 80-lead LQFP surface-mount packaging
- Three modes of operation:
  - Quadrature modulator mode
  - Single-tone mode
  - Interpolating DAC mode

APPLICATIONS

- HFC data, telephony, and video modems
- Wireless base station
- Agile, LO frequency synthesis
- Broadband communications

FUNCTIONAL BLOCK DIAGRAM

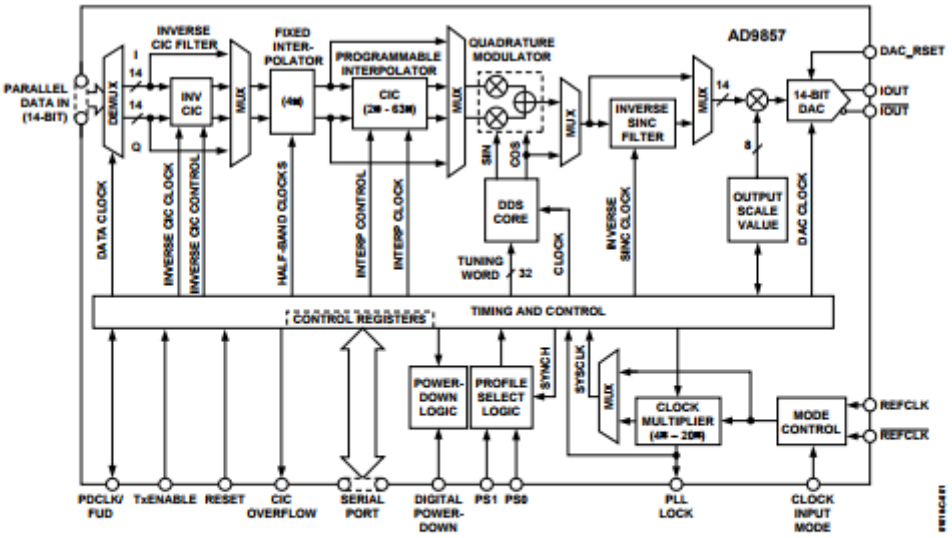

Figure 1.

SPECIFICATIONS

V_S = 3.3 V ± 5%, R_{SET} = 1.96 kΩ, external reference clock frequency = 10 MHz with REFCLK multiplier enabled at 20×.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	1		200	MHz
REFCLK Multiplier Enabled at 4×	Full	VI	1		50	MHz
REFCLK Multiplier Enabled at 20×	Full	VI	1		10	MHz
Input Capacitance	25°C	V		3		pF
Input Impedance	25°C	V		100		MΩ
Duty Cycle	25°C	V		50		%
Duty Cycle with REFCLK Multiplier Enabled	25°C	V	35		65	%
Differential Input (VDD/2) ±200 mV	25°C	V	1.45		1.85	V
DAC OUTPUT CHARACTERISTICS						
Resolution				14		Bits
Full-Scale Output Current			5	10	20	mA
Gain Error	25°C	I	8.5		0	% FS
Output Offset	25°C	I			2	µA
Differential Nonlinearity	25°C	V		1.6		LSB
Integral Nonlinearity	25°C	V		2		LSB
Output Capacitance	25°C	V		5		pF
Residual Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}						
REFCLK Multiplier Enabled at 20×	25°C	V		−107		dBc/Hz
REFCLK Multiplier at 4×	25°C	V		−123		dBc/Hz
REFCLK Multiplier Disabled	25°C	V		−145		dBc/Hz
Voltage Compliance Range	25°C	I	−0.5		+1.0	V
Wideband SFDR						
1 MHz to 20 MHz Analog Out	25°C	V		−75		dBc
20 MHz to 40 MHz Analog Out	25°C	V		−65		dBc
40 MHz to 60 MHz Analog Out	25°C	V		−62		dBc
60 MHz to 80 MHz Analog Out	25°C	V		−60		dBc
Narrowband SFDR						
10 MHz Analog Out (±1 MHz)	25°C	V		−87		dBc
10 MHz Analog Out (±250 kHz)	25°C	V		−88		dBc
10 MHz Analog Out (±50 kHz)	25°C	V		−92		dBc
10 MHz Analog Out (±10 kHz)	25°C	V		−94		dBc
65 MHz Analog Out (±1 MHz)	25°C	V		−86		dBc
65 MHz Analog Out (±250 kHz)	25°C	V		−86		dBc
65 MHz Analog Out (±50 kHz)	25°C	V		−86		dBc
65 MHz Analog Out (±10 kHz)	25°C	V		−88		dBc
80 MHz Analog Out (±1 MHz)	25°C	V		−85		dBc
80 MHz Analog Out (±250 kHz)	25°C	V		−85		dBc
80 MHz Analog Out (±50 kHz)	25°C	V		−85		dBc
80 MHz Analog Out (±0 kHz)	25°C	V		−86		dBc

Parameter	Temp	Test Level	Min	Typ	Max	Unit
MODULATOR CHARACTERISTICS (65 MHz A_{OUT})						
(Input data: 2.5 MS/s, QPSK, 4× oversampled, inverse SINC filter ON, inverse CIC ON)						
I/Q Offset	25°C	IV	55	65		dB
Error Vector Magnitude	25°C	IV		0.4	1	%
INVERSE SINC FILTER (variation in gain from DC to 80 MHz, inverse SINC filter ON)	25°C	V		±0.1		dB
SPURIOUS POWER (off channel, measured in equivalent bandwidth), Full-Scale Output						
6.4 MHz Bandwidth	25°C	IV		−65		dBc
3.2 MHz Bandwidth	25°C	IV		−67		dBc
1.6 MHz Bandwidth	25°C	IV		−69		dBc
0.8 MHz Bandwidth	25°C	IV		−69		dBc
0.4 MHz Bandwidth	25°C	IV		−70		dBc
0.2 MHz Bandwidth	25°C	IV		−72		dBc
SPURIOUS POWER (Off channel, measured in equivalent bandwidth), Output Attenuated 18 dB						
Relative to Full Scale						
6.4 MHz Bandwidth	25°C	IV		−51		dBc
3.2 MHz Bandwidth	25°C	IV		−54		dBc
1.6 MHz Bandwidth	25°C	IV		−56		dBc
0.8 MHz Bandwidth	25°C	IV		−59		dBc
0.4 MHz Bandwidth	25°C	IV		−62		dBc
0.2 MHz Bandwidth	25°C	IV		−63		dBc
TIMING CHARACTERISTICS						
Serial Control Bus						
Maximum Frequency	25°C	I			10	MHz
Minimum Clock Pulse Width Low (t_{PWL})	25°C	I	30			ns
Minimum Clock Pulse Width High (t_{PWH})	25°C	I	30			ns
Maximum Clock Rise/Fall Time	25°C	I			1	ms
Minimum Data Setup Time (t_{DS})	25°C	I	30			ns
Minimum Data Hold Time (t_{DH})	25°C	I	0			ns
Maximum Data Valid Time (t_{DV})	25°C	I	35			ns
Wake-Up Time[1]	25°C	I		1		ms
Minimum RESET Pulse Width High (t_{RH})	25°C	I	5			SYSCLK[2]2Cycles
Minimum $\overline{CS}$ Setup Time	25°C	I	40			ns
CMOS LOGIC INPUTS						
Logic 1 Voltage	25°C	IV	2.0			V
Logic 0 Voltage	25°C	IV			0.8	V
Logic 1 Current	25°C	I			5	µA
Logic 0 Current	25°C	I			5	µA
Input Capacitance	25°C	V		3		pF
CMOS LOGIC OUTPUTS (1 mA LOAD)						
Logic 1 Voltage	25°C	I	2.7			V
Logic 0 Voltage	25°C	I			0.4	V

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Parameter	Temp	Test Level	Min	Typ	Max	Unit
POWER SUPPLY V_SCURRENT[3] (all power specifications at V_{DD} = 3.3 V, 25°C, REFCLK = 200 MHz)						
Full Operating Conditions	25°C	I		540	615	mA
160 MHz Clock (×16)	25°C	I		445	515	mA
120 MHz Clock (×12)	25°C	I		345	400	mA
Burst Operation (25%)	25°C	I		395	450	mA
Single-Tone Mode	25°C	I		265	310	mA
Power-Down Mode	25°C	I		71	80	mA
Full-Sleep Mode	25°C	I		8	13.5	mA

[1] Wake-up time refers to recovery from full-sleep mode. The longest time required is for the reference clock multiplier PLL to lock up (if it is being used). The wake-up time assumes that there is no capacitor on DAC_BP, and that the recommended PLL loop filter values are used. The state of the reference clock multiplier lock can be determined by observing the signal on the PLL_LOCK pin.

[2] SYSCLK refers to the actual clock frequency used on-chip by the AD9857. If the reference clock multiplier is used to multiply the external reference frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplier multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external REFCLK frequency.

[3] CIC = 2, INV SINC ON, FTW = 40%, PLL OFF, auto power-down between burst On, TxENABLE duty cycle = 25%.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
V_S	4 V
Digital Input Voltage	−0.7 V to +V_S
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Lead Temperature (Soldering 10 s)	300°C
θ_{JA}	35°C/W
θ_{JC}	16°C/W

EXPLANATION OF TEST LEVELS

Table 3.

Test	Level
1	100% production tested.
2	100% production tested at 25°C and sample tested at specific temperatures.
3	Sample tested only.
4	Parameter is guaranteed by design and characterization testing.
5	Parameter is a typical value only.
6	Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

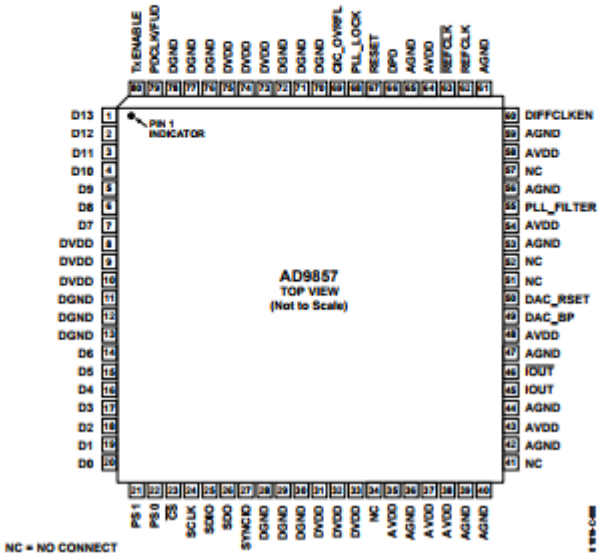

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin Number	Mnemonic	I/O	Function
20–14, 7–1	D0–D6, D7–D13	I	14-Bit Parallel Data Bus for I and Q Data. The required numeric format is twos complement with D13 as the sign bit and D12–D0 as the magnitude bits. Alternating 14-bit words are demultiplexed onto the I and Q data pathways (except when operating in the interpolating DAC mode, in which case every word is routed onto the I data path). When the TxENABLE pin is asserted high, the next accepted word is presumed to be I data, the next Q data, and so forth.
8–10, 31–33, 73–75	DVDD		3.3 V Digital Power pin(s).
11–13, 28–30, 70–72, 76–78	DGND		Digital Ground pin(s).
21	PS1	I	Profile Select Pin 1. The LSB of the two profile select pins. In conjunction with PS0, selects one of four profile configurations.
22	PS0	I	Profile Select Pin 0. The MSB of the two profile select pins. In conjunction with P1, selects one of four profile configurations.
23	$\overline{CS}$	I	Serial Port Chip Select pin. An active low signal that allows multiple devices to operate on a single serial bus.
24	SCLK	I	Serial Port Data Clock pin. The serial data CLOCK for the serial port.
25	SDIO	I/O	Serial Port Input/Output Data pin. Bidirectional serial DATA pin for the serial port. This pin can be programmed to operate as a serial *input only* pin, via the control register bit 00h<7>. The default state is bidirectional.
26	SDO	O	Serial Port Output Data pin. This pin serves as the serial data output pin when the SDIO pin is configured for serial input only mode. The default state is three-state.
27	SYNCIO	I	Serial Port Synchronization pin. Synchronizes the serial port without affecting the programmable register contents. This is an active high input that aborts the current serial communication cycle.
34, 41, 51, 52, 57	NC		No connect.

Pin Number	Mnemonic	I/O	Function
35, 37, 38, 43, 48, 54, 58, 64	AVDD		3.3 V Analog Power pin(s).
36, 39, 40, 42, 44, 47, 53, 56, 59, 61, 65	AGND		Analog Ground pin(s).
45	IOUT	O	DAC Output pin. Normal DAC output current (analog).
46	$\overline{\text{IOUT}}$	O	DAC Complementary Output pin. Complementary DAC output current (analog).
49	DAC_BP		DAC Reference Bypass. Typically not used.
50	DAC_RSET	I	DAC Current Set pin. Sets DAC reference current.
55	PLL_FILTER	O	PLL Filter. R-C network for PLL filter.
60	DIFFCLKEN	I	Clock Mode Select pin. A logic high on this pin selects DIFFERENTIAL REFCLK input mode. A logic low selects the SINGLE-ENDED REFCLK input mode.
62	REFCLK	I	Reference Clock pin. In single-ended clock mode, this pin is the Reference Clock input. In differential clock mode, this pin is the positive clock input.
63	$\overline{\text{REFCLK}}$	I	Inverted Reference Clock pin. In differential clock mode, this pin is the negative clock input.
66	DPD	I	Digital Power-Down pin. Assertion of this pin shuts down the digital sections of the device to conserve power. However, if selected, the PLL remains operational.
67	RESET	I	Hardware RESET pin. An active high input that forces the device into a predefined state.
68	PLL_LOCK	O	PLL Lock pin. Active high output signifying, in real time, when PLL is in lock state.
69	CIC_OVRFL	O	CIC Overflow pin. Activity on this pin indicates that the CIC Filters are in "overflow" state. This pin is typically low unless a CIC overflow occurs.
79	PDCLK/FUD	I/O	Parallel Data Clock/Frequency Update pin. When not in single-tone mode, this pin is an output signal that should be used as a clock to synchronize the acceptance of the 14-bit parallel data-words on Pins D13–D0. In single-tone mode, this pin is an input signal that synchronizes the transfer of a changed frequency tuning word (FTW) in the active profile (PSx) to the accumulator (FUD = frequency update signal). When profiles are changed by means of the PS–PS1 pins, the FUD does not have to be asserted to make the FTW active.
80	TxENABLE	I	When TxENABLE is asserted, the device processes the data through the I and Q data pathways; otherwise 0s are internally substituted for the I and Q data entering the signal path. The first data word accepted when the TxENABLE is asserted high is treated as I data, the next data word is Q data, and so forth.

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TYPICAL PERFORMANCE CHARACTERISTICS

MODULATED OUTPUT SPECTRAL PLOTS

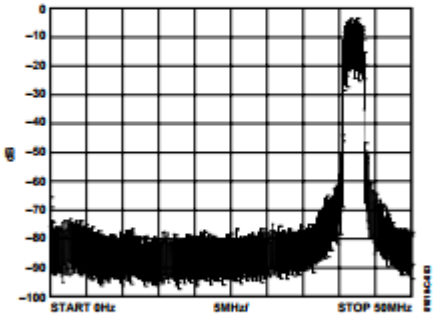

Figure 3. QPSK at 42 MHz and 2.56 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 12, CIC Interpolation Rate = 3, 4× Oversampled Data

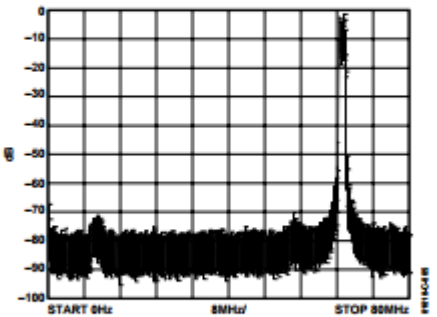

Figure 5. 16-QAM at 65 MHz and 1.28 MS/s; 10.24 MHz External Clock with REFCLK Multiplier = 18, CIC Interpolation Rate = 9, 4× Oversampled Data

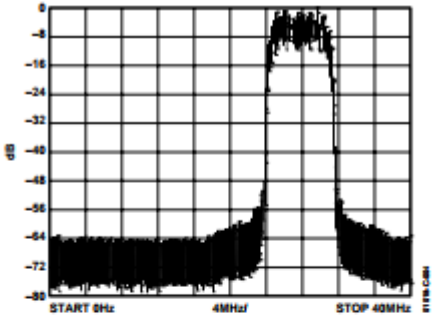

Figure 4. 64-QAM at 28 MHz and 6 MS/s; 36 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 3× Oversampled Data

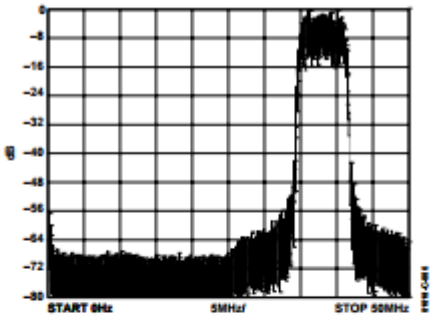

Figure 6. 256-QAM at 38 MHz and 6 MS/s; 48 MHz External Clock with REFCLK Multiplier = 4, CIC Interpolation Rate = 2, 4× Oversampled Data

MODES OF OPERATION

The AD9857 has three operating modes:

- Quadrature modulation mode (default)
- Single-tone mode
- Interpolating DAC mode

Mode selection is accomplished by programming a control register via the serial port. The inverse SINC filter and output scale multiplier are available in all three modes.

QUADRATURE MODULATION MODE

In quadrature modulation mode, both the I and Q data paths are active. A block diagram of the AD9857 operating in the quadrature modulation mode is shown in Figure 18.

In quadrature modulation mode, the PDCLK/FUD pin is an output and functions as the parallel data clock (PDCLK), which serves to synchronize the input of data to the AD9857. In this mode, the input data must be synchronized with the rising edge of PDCLK. The PDCLK operates at *twice* the rate of either the I or Q data path. This is due to the fact that the I and Q data must be presented to the parallel port as two 14-bit words multiplexed in time. One I word and one Q word together comprise one internal *sample*. Each sample is propagated along the internal data pathway in parallel fashion.

The DDS core provides a quadrature (sin and cos) local oscillator signal to the quadrature modulator, where the I and Q data are multiplied by the respective phase of the carrier and summed together, to produce a quadrature-modulated data stream.

All of this occurs in the digital domain, and only then is the digital data stream applied to the 14-bit DAC to become the quadrature-modulated analog output signal.

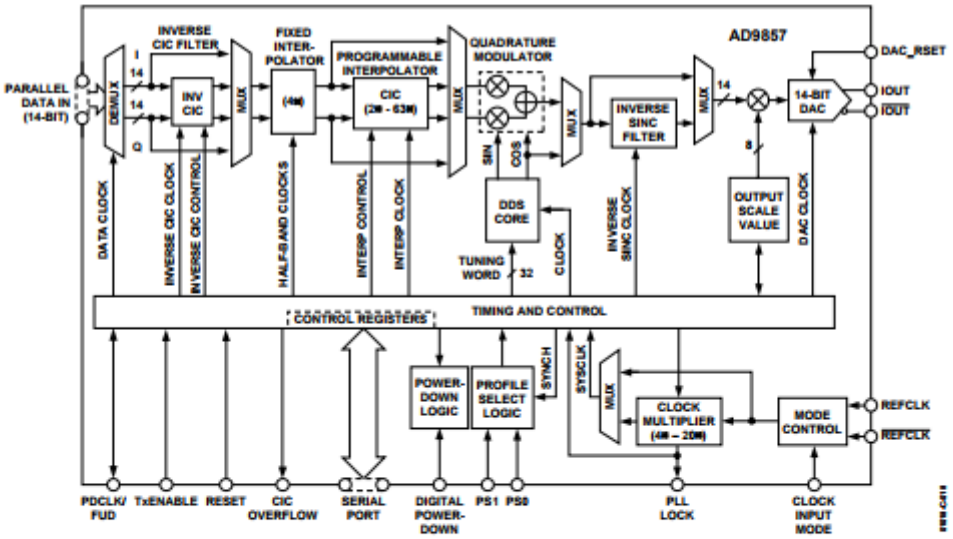

Figure 18. Quadrature Modulation Mode

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SINGLE-TONE MODE

A block diagram of the AD9857 operating in the single-tone mode is shown in Figure 19. In the single-tone mode, both the I and Q data paths are disabled from the 14-bit parallel data port up to and including the modulator. The PDCLK/ FUD pin is an input and functions as a frequency update (FUD) control signal. This is necessary because the frequency tuning word is programmed via the asynchronous serial port. The FUD signal causes the new frequency tuning word to become active.

In single-tone mode, the cosine portion of the DDS serves as the signal source. The output signal consists of a single frequency as determined by the tuning word stored in the appropriate control register, per each profile.

In the single-tone mode, no 14-bit parallel data is applied to the AD9857. The internal DDS core is used to produce a single frequency signal according to the tuning word. The single-tone signal then moves toward the output, where the inverse SINC filter and the output scaling can be applied. Finally, the digital single-tone signal is converted to the analog domain by the 14-bit DAC.

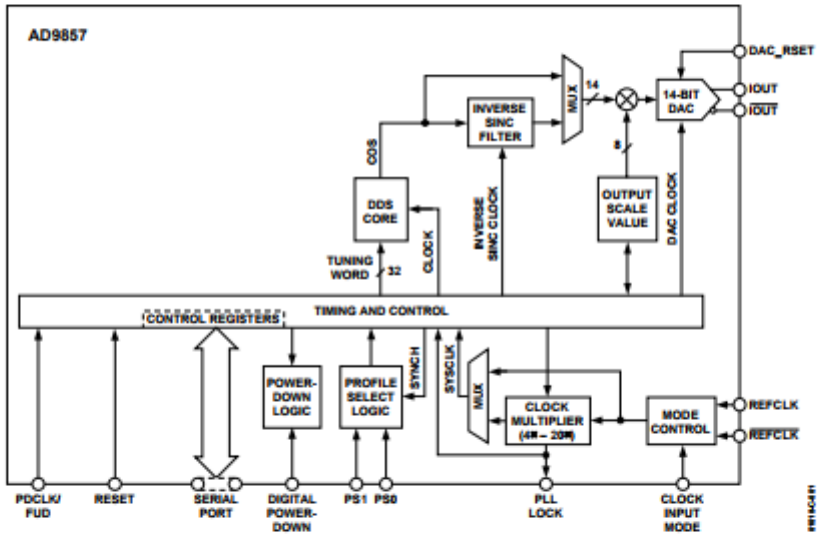

Figure 19. Single-Tone Mode