74AC377, 74ACT377
Octal D-Type Flip-Flop with Clock Enable

Features

- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Outputs source/sink 24mA
- See 273 for master reset version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- ACT377 has TTL-compatible inputs

General Description

The AC/ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.
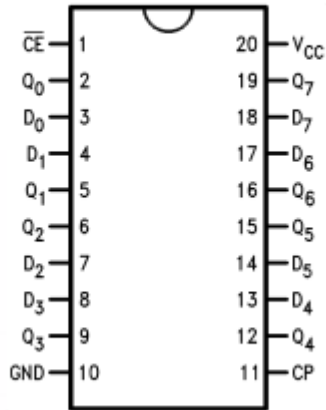
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Ordering Information

Order Number	Package Number	Package Description
74AC377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT377MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
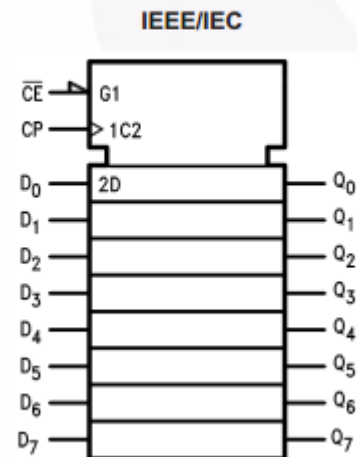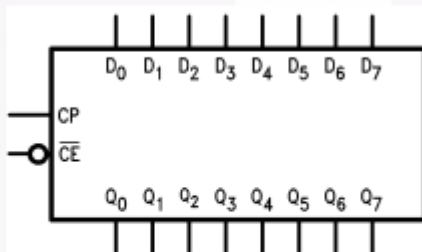
Connection Diagram

$\overline{CE}$	1	20	V_{CC}
Q_0	2	19	Q_7
D_0	3	18	D_7
D_1	4	17	D_6
Q_1	5	16	Q_6
Q_2	6	15	Q_5
D_2	7	14	D_5
D_3	8	13	D_4
Q_3	9	12	Q_4
GND	10	11	CP

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Logic Symbols

IEEE/IEC

Mode Select-Function Table

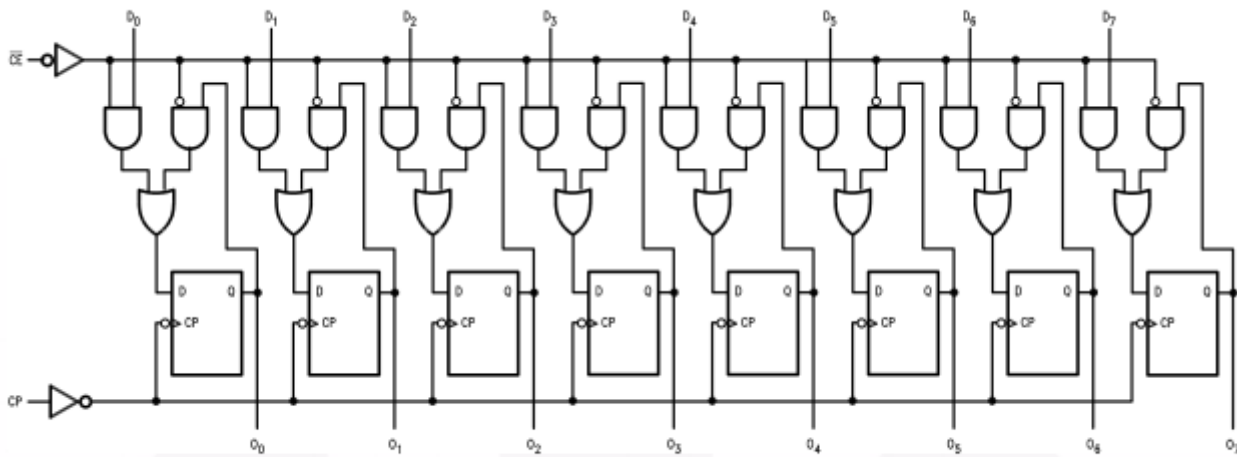|	Inputs			Outputs
Operating Mode	**CP**	**$\overline{CE}$**	**D_n**	**Q_n**
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	−0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	−0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

DC Electrical Characteristics for AC

Symbol	Parameter	Vcc (V)	Conditions	TA = +25°C Typ.	Guaranteed Limits	TA = −40°C to +85°C	Units
V_{IH}	Minimum HIGH Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	$I_{OUT} = -50\mu A$	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -12mA$		2.56	2.46	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA^{(1)}$		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	$I_{OUT} = 50\mu A$	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 12mA$		0.36	0.44	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA^{(1)}$		0.36	0.44	
$I_{IN}^{(3)}$	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	µA
I_{OLD}	Minimum Dynamic Output Current$^{(2)}$	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}			$V_{OHD} = 3.85V$ Min.			−75	mA
$I_{CC}^{(3)}$	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.

2. Maximum test duration 2.0ms, one output loaded at a time.

3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	Vcc (V)	Conditions	TA = +25°C Typ.	TA = +25°C Guaranteed Limits	TA = −40°C to +85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA^{(4)}$		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA^{(4)}$		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	± 1.0	µA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current[5]	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}			$V_{OHD} = 3.85V$ Min.			−75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	µA

Notes:
4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	Vcc (V)[6]	TA = +25°C Min.	TA = +25°C Typ.	TA = +25°C Max.	TA = −40°C to +85°C Min.	TA = −40°C to +85°C Max.	Units
f_{MAX}	Maximum Clock Frequency	3.3	90	125		75		MHz
		5.0	140	175		125		
t_{PLH}	Propagation Delay, CP to Q_n	3.3	3.0	8.0	13.0	1.5	14.0	ns
		5.0	2.0	6.0	9.0	1.5	10.0	
t_{PHL}	Propagation Delay, CP to Q_n	3.3	3.5	8.5	13.0	2.0	14.5	ns
		5.0	2.5	6.5	10.0	1.5	11.0	

Note:
6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V)[7]	$T_A = +25°C$, $C_L = 50pF$ Typ.	$T_A = +25°C$, $C_L = 50pF$ Guaranteed Minimum	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$ Guaranteed Minimum	Units
t_S	Setup Time, HIGH or LOW, D_n to CP	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
t_H	Hold Time, HIGH or LOW, D_n to CP	3.3	−2.0	0	0	ns
		5.0	−1.0	1.0	1.0	
t_S	Setup Time, HIGH or LOW, $\overline{CE}$ to CP	3.3	4.0	6.0	7.5	ns
		5.0	2.5	4.0	4.5	
t_H	Hold Time, HIGH or LOW, $\overline{CE}$ to CP	3.3	−3.5	0	0	ns
		5.0	−2.0	1.0	1.0	
t_W	CP Pulse Width, HIGH or LOW	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

Note:
7. Voltage range 3.3 is 3.0V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[8]	$T_A = +25°C$, $C_L = 50pF$ Min.	Typ.	Max.	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$ Min.	Max.	Units
f_{MAX}	Maximum Clock Frequency	5.0	140	175		125		MHz
t_{PLH}	Propagation Delay, CP to Q_n	5.0	3.0	6.5	9.0	2.5	10.0	ns
t_{PHL}	Propagation Delay, CP to Q_n	5.0	3.5	7.0	10.0	2.5	11.0	ns

Note:
8. Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

Symbol	Parameter	V_{CC} (V)[9]	$T_A = +25°C$, $C_L = 50pF$ Typ.	$T_A = +25°C$, $C_L = 50pF$ Guaranteed Minimum	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$ Guaranteed Minimum	Units
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	2.5	4.5	5.5	ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	−1.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW, $\overline{CE}$ to CP	5.0	2.5	4.5	5.5	ns
t_H	Hold Time, HIGH or LOW, $\overline{CE}$ to CP	5.0	−1.0	1.0	1.0	ns
t_W	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.5	ns

Note:
9. Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	90.0	pF