LP3853/LP3856 3A Fast Response Ultra Low Dropout Linear Regulators

Check for Samples: LP3853, LP3856

FEATURES

- Ultra Low Dropout Voltage
- Stable with Selected Ceramic Capacitors
- Low Ground Pin Current
- Load Regulation of 0.08%
- 10nA Quiescent Current in Shutdown Mode
- Ensured Output Current of 3A DC
- Available in TO-263 and TO-220 Packages
- Output Voltage Accuracy ± 1.5%
- Error Flag Indicates Output Status
- Sense Option Improves Load Regulation
- Overtemperature/overcurrent Protection
- −40°C to +125°C Junction Temperature Range

APPLICATIONS

- Microprocessor Power Supplies
- Stable with Ceramic Output Capacitors
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- High Efficiency Linear Regulators
- Battery Chargers
- Other Battery Powered Applications

DESCRIPTION

The LP3853/LP3856 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3853/LP3856 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3853/LP3856 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 39mV at 300mA load current and 390mV at 3A load current.

Ground Pin Current: Typically 4mA at 3A load current.

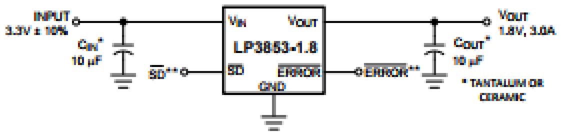
Shutdown Mode: Typically 10nA quiescent current when the shutdown pin is pulled low.

Error Flag: Error flag goes low when the output voltage drops 10% below nominal value.

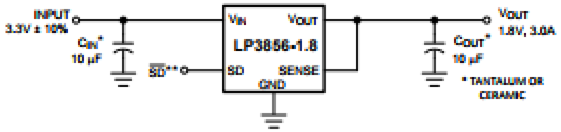
SENSE: Sense pin improves regulation at remote loads.

Precision Output Voltage: Multiple output voltage options are available ranging from 1.8V to 5.0V with a ensured accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

Typical Application Circuits



**SD and ERROR pins must be pulled high through a 10kΩ pull-up resistor. Connect the ERROR pin to ground if this function is not used. See Application Hints for more information.



**SD pin must be pulled high through a 10kΩ pull-up resistor. See Application Hints for more information.

Connection Diagram

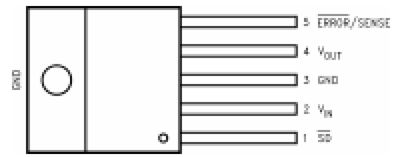


Figure 1. Top View
TO220-5 Package
Bent, Staggered Leads

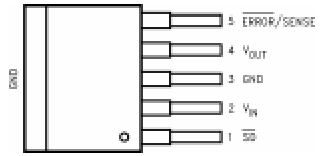


Figure 2. Top View
TO263-5 Package

Table 1. Pin Description for TO220-5 and TO263-5 Packages

Pin #	LP3853		LP3856	
	Name	Function	Name	Function
1	SD	Shutdown	SD	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	ERROR	ERROR Flag	SENSE	Remote Sense Pin

Block Diagram

LP3853

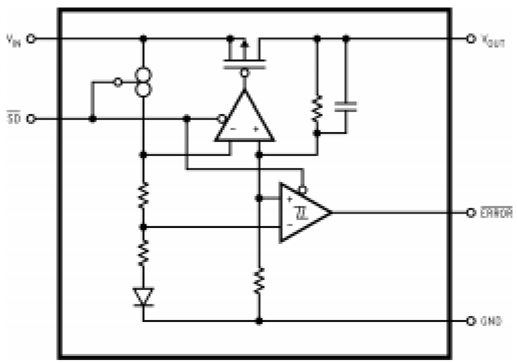


Figure 3.

LP3856

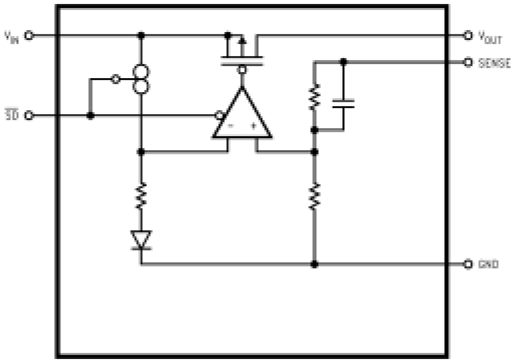


Figure 4.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [(1)]

Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 5 sec.)	260°C
ESD Rating [(2)]	2 kV
Power Dissipation [(3)]	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +7.5V
Shutdown Input Voltage (Survival)	−0.3V to 7.5V
Output Voltage (Survival), [(4)], [(5)]	−0.3V to +6.0V
I_{OUT} (Survival)	Short Circuit Protected
Maximum Voltage for $\overline{ERROR}$ Pin	V_{IN}
Maximum Voltage for SENSE Pin	V_{OUT}

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ_{JA} = 50°C/W (with 0.5in², 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at θ_{JA} = 60°C/W (with 0.5in², 1oz. copper area), junction-to-ambient. See Application Hints.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
(5) The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

Operating Ratings

Input Supply Voltage [(1)]	2.5V to 7.0V
Shutdown Input Voltage	−0.3V to 7.0V
Maximum Operating Current (DC)	3A
Junction Temperature	−40°C to +125°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5V, whichever is greater.

Electrical Characteristics LP3853/LP3856

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: V_{IN} = $V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} = 10µF, V_{SD} = 2V.

Symbol	Parameter	Conditions	Typ [(1)]	LP3853/6 [(2)]		Units
				Min	Max	
V_O	Output Voltage Tolerance (3)	V_{OUT} +1V ≤ V_{IN} ≤ 7.0V 10 mA ≤ I_L ≤ 3A	0	-1.5 **-3.0**	+1.5 **+3.0**	%
ΔV_{OL}	Output Voltage Line Regulation (3)	V_{OUT} +1V ≤ V_{IN} ≤ 7.0V	0.02 **0.06**			%
$\Delta V_O/\Delta I_{OUT}$	Output Voltage Load Regulation (3)	10 mA ≤ I_L ≤ 3A	0.08 **0.14**			%
V_{IN} - V_{OUT}	Dropout Voltage (4)	I_L = 300 mA	39		50 **65**	mV
		I_L = 3A	390		450 **600**	
I_{GND}	Ground Pin Current In Normal Operation Mode	I_L = 300 mA	4		9 **10**	mA
		I_L = 3A	4		9 **10**	
I_{GND}	Ground Pin Current In Shutdown Mode	V_{SD} ≤ 0.3V	0.01		10	µA
		-40°C ≤ T_J ≤ 85°C			**50**	
$I_{O(PK)}$	Peak Output Current	V_O ≥ $V_{O(NOM)}$ - 4%	4.5			A
Short Circuit Protection						
I_{SC}	Short Circuit Current		6			A
Shutdown Input						
V_{SDT}	Shutdown Threshold	V_{SDT} Rising from 0.3V until Output = ON	1.3	2		V
		V_{SDT} Falling from 2.0V until Output = OFF	1.3		0.3	
T_{dOFF}	Turn-off delay	I_L = 3A	20			µs
T_{dON}	Turn-on delay	I_L = 3A	25			µs
I_{SD}	$\overline{SD}$ Input Current	V_{SD} = V_{IN}	1			nA
Error Flag						
V_T	Threshold	(5)	10	5	16	%
V_{TH}	Threshold Hysteresis	(5)	5	2	8	%
$V_{EF(Sat)}$	$\overline{Error}$ Flag Saturation	I_{sink} = 100µA	0.02		0.1	V
Td	Flag Reset Delay		1			µs
I_{lk}	$\overline{Error}$ Flag Pin Leakage Current		1			nA
I_{max}	$\overline{Error}$ Flag Pin Sink Current	V_{Error} = 0.5V	1			mA

(1) Typical numbers are at 25°C and represent the most likely parametric norm.
(2) Limits are ensured by testing, design, or statistical correlation.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.
(5) $\overline{Error}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage. See Application Hints.

Electrical Characteristics LP3853/LP3856 (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} = 10µF, V_{SD} = 2V.

Symbol	Parameter	Conditions	Typ [1]	LP3853/6 [2]		Units
				Min	Max	
AC Parameters						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1V C_{OUT} = 10uF V_{OUT} = 3.3V, f = 120Hz	73			dB
		$V_{IN} = V_{OUT}$ + 0.5V C_{OUT} = 10uF V_{OUT} = 3.3V, f = 120Hz	57			
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz	0.8			µV
e_n	Output Noise Voltage	BW = 10Hz – 100kHz V_{OUT} = 2.5V	150			µV (rms)
		BW = 300Hz – 300kHz V_{OUT} = 2.5V	100			

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA.

Dropout Voltage vs Output Load Current

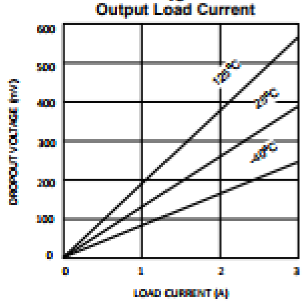


Figure 5.

Ground Current vs Output Load Current V_{OUT} = 5V

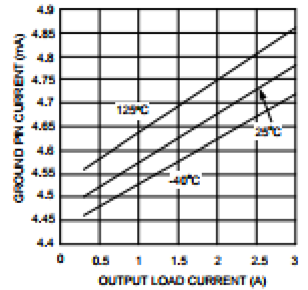


Figure 6.

Ground Current vs Output Voltage IL = 3A

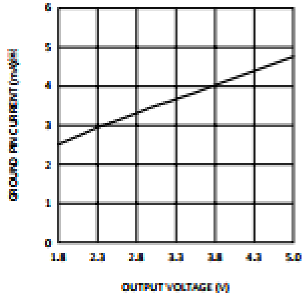


Figure 7.

Shutdown I_Q vs Junction Temperature

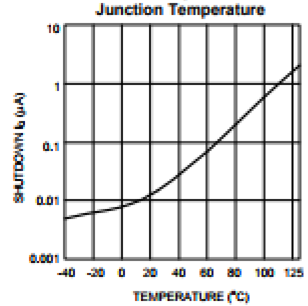


Figure 8.

Errorflag Threshold vs Junction Temperature

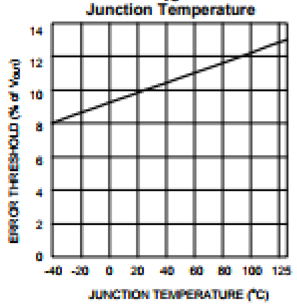


Figure 9.

DC Load Reg. vs Junction Temperature

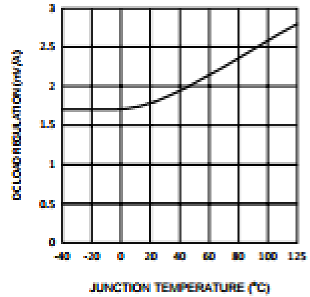


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA.

DC Line Regulation vs Temperature

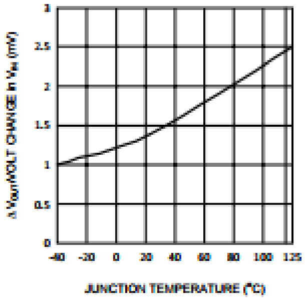


Figure 11.

V_{IN} vs V_{OUT} Over Temperature

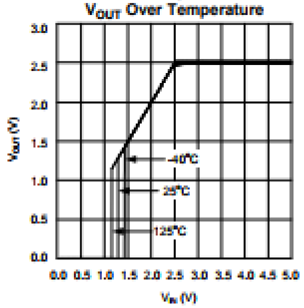


Figure 12.

Noise vs Frequency

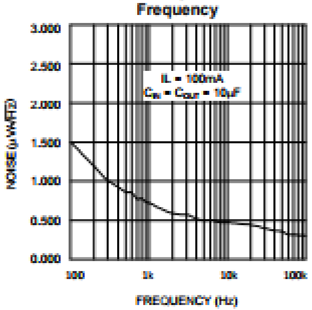


Figure 13.

Load Transient Response $C_{IN} = C_{OUT}$ = 10µF, OSCON

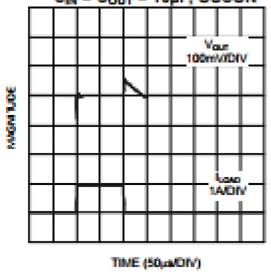


Figure 14.

Load Transient Response $C_{IN} = C_{OUT}$ = 100µF, OSCON

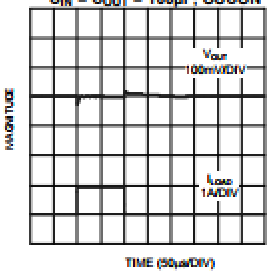


Figure 15.

Load Transient Response $C_{IN} = C_{OUT}$ = 100µF, POSCAP

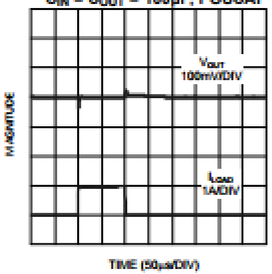


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA.

Load Transient Response $C_{IN} = C_{OUT}$ = 10µF, TANTALUM

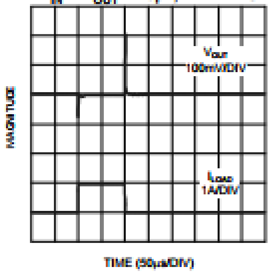


Figure 17.

Load Transient Response $C_{IN} = C_{OUT}$ = 100µF, TANTALUM

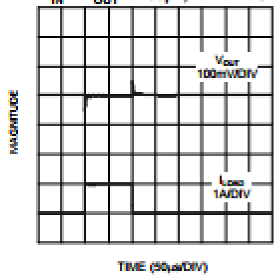


Figure 18.

Load Transient Response $C_{IN} = C_{OUT}$ = 10µF, OSCON

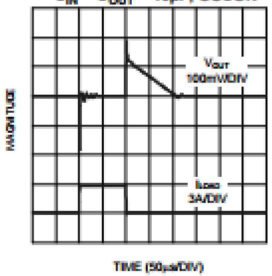


Figure 19.

Load Transient Response $C_{IN} = C_{OUT}$ = 100µF, OSCON

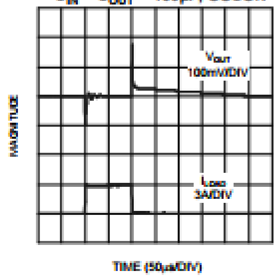


Figure 20.

Load Transient Response $C_{IN} = C_{OUT}$ = 100µF, POSCAP

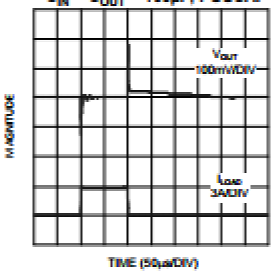


Figure 21.

Load Transient Response $C_{IN} = C_{OUT}$ = 10µF, TANTALUM

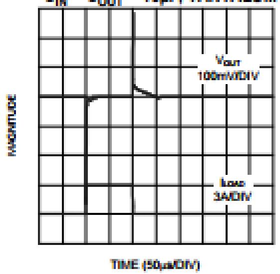


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10µF, C_{IN} = 10µF, S/D pin is tied to V_{IN}, V_{OUT} = 2.5V, $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA.

Load Transient Response
$C_{IN} = C_{OUT}$ = 100µF, TANTALUM

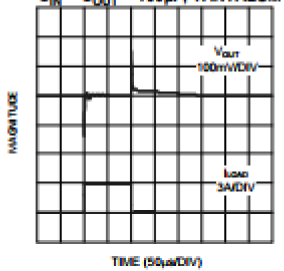


Figure 23.

Load Transient Response
C_{IN} = 4 x 10µF CERAMIC, C_{OUT} = 3 x 10µF CERAMIC

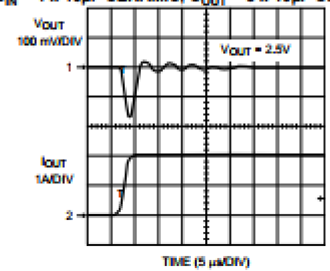


Figure 24.

Load Transient Response
C_{IN} = 4 x 10µF CERAMIC, C_{OUT} = 3 x 10µF CERAMIC

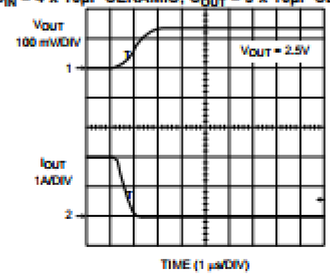


Figure 25.

Load Transient Response
C_{IN} = 2 x 10µF CERAMIC, C_{OUT} = 2 x 10µF CERAMIC

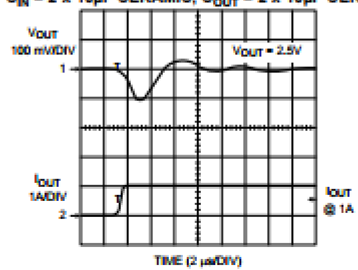


Figure 26.

Load Transient Response
C_{IN} = 2 x 10µF CERAMIC, C_{OUT} = 2 x 10µF CERAMIC

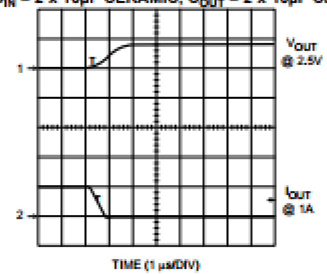


Figure 27.

APPLICATION INFORMATION

Application Hints

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor of at least 10µF is required. Ceramic or Tantalum may be used, and capacitance may be increased without limit

OUTPUT CAPACITOR: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum amount of output capacitance that can be used for stable operation is 10µF. For general usage across all load currents and operating conditions, the part was characterized using a 10µF Tantalum input capacitor. The minimum and maximum stable ESR range for the output capacitor was then measured which kept the device stable, assuming any output capacitor whose value is greater than 10µF (see Figure 28 below).

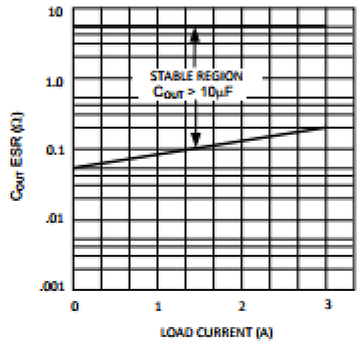


Figure 28. ESR Curve for C_{OUT} (with 10µF Tantalum Input Capacitor)

It should be noted that it is possible to operate the part with an output capacitor whose ESR is below these limits, assuming that sufficient ceramic input capacitance is provided. This will allow stable operation using ceramic output capacitors (see next section).

OPERATION WITH CERAMIC OUTPUT CAPACITORS

LP385X voltage regulators can operate with ceramic output capacitors if the values of input and output capacitors are selected appropriately. The total ceramic output capacitance must be equal to or less than a specified maximum value in order for the regulator to remain stable over all operating conditions. This maximum amount of ceramic output capacitance is dependent upon the amount of ceramic input capacitance used as well as the load current of the application. This relationship is shown in Figure 29, which graphs the maximum stable value of ceramic output capacitance as a function of ceramic input capacitance for load currents of 1A, 2A, and 3A. For example, if the maximum load current is 1A, a 10µF ceramic input capacitor will allow stable operation for values of ceramic output capacitance from 10µF up to about 500µF.