# LP2989 Micropower and Low-Noise, 500-mA Ultra Low-Dropout Regulator for Use With Ceramic Output Capacitors

## 1 Features

- 2.1-V to 16-V Input Voltage Range
- 2.5-V to 5-V Fixed Output Voltage Options
- Ultra-Low Dropout Voltage
- 500-mA Continuous Output Current
- Very Low Output Noise With External Capacitor
- < 0.8-µA Quiescent Current When Shutdown
- Low Ground Pin Current at All Loads
- 0.75% Output Voltage Accuracy (A Grade)
- High Peak Current Capability (800-mA typical)
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

## 2 Applications

- Notebooks and Desktop PCs
- PDAs and Palmtop Computers
- Wireless Communication Pins
- SMPS Post-Regulators

## 3 Description

The LP2989 is a fixed-output 500-mA precision LDO regulator designed for use with ceramic output capacitors.

Output noise can be reduced to 18 µV (typical) by connecting an external 10-nF capacitor to the bypass pin.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2989 delivers superior performance:

- **Dropout Voltage:** Typically 310 mV at 500-mA load, and 1 mV at 100-µA load.
- **Ground Pin Current:** Typically 3 mA at 500-mA load, and 110 µA at 100-µA load.
- **Sleep Mode:** The LP2989 draws less than 0.8-µA quiescent current when $\overline{\text{SHUTDOWN}}$ pin is pulled low.
- **Error Flag:** The built-in error flag goes low when the output drops approximately 5% below nominal.
- **Precision Output:** Output voltage accuracy is 0.75% (A grade) and 1.25% (standard grade) at room temperature.

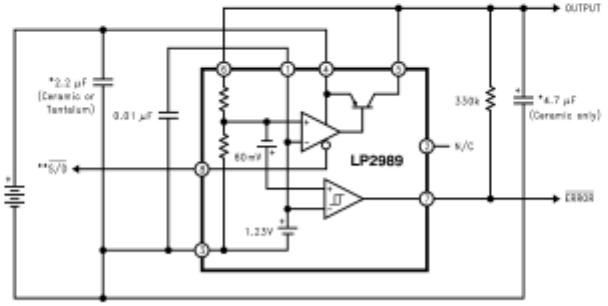
For output voltages < 2 V, see LP2989LV (SNVS086) data sheet.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LP2989 | WSON (8) | 4.00 mm x 4.00 mm |
| | SOIC (8) | 4.90 mm x 3.91 mm |
| | VSSOP (8) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application**

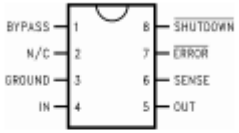



*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. See the *Output Capacitor* section.

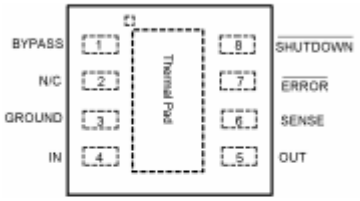
**Shutdown must be actively terminated (see the *Shutdown Input Operation* section). Tie to IN (pin 4) if not use.

## 5 Pin Configuration and Functions

**D/DGK Packages**
**8-Pin SOIC and VSSOP**
**Top View**




**NGN Package**
**8-Lead WSON**
**Top View**




**Pin Functions**

| PIN NAME | PIN NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BYPASS | 1 | I | Bypass capacitor input |
| $\overline{\text{ERROR}}$ | 7 | O | Error signal output |
| GROUND | 3 | — | GND |
| INPUT | 4 | I | Regulator power input |
| N/C | 2 | — | DO NOT CONNECT. Device pin 2 is reserved for post packaging test and calibration of the LP2989 $V_{OUT}$ accuracy. Device pin 2 must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 2 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 2 may activate the trim circuitry forcing $V_{OUT}$ to move out of tolerance. |
| OUTPUT | 5 | O | Regulated output voltage |
| SENSE | 6 | I | Feedback voltage sense input |
| $\overline{\text{SHUTDOWN}}$ | 8 | I | Shutdown input |
| Thermal Pad | — | — | The exposed thermal pad on the bottom of the WSON package should be connected to a copper thermal pad on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3. For additional information on using TI's Non Pull Back WSON package, see Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401). |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

If Military/Aerospace specified devices are required contact the Texas Instruments Sales Office/Distributors for availability and specifications.(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Operating junction temperature | | –40 | 125 | °C |
| Power dissipation(2) | | Internally Limited | | |
| Input supply voltage | Survival | –0.3 | 16 | V |
| SENSE pin | | –0.3 | 6 | V |
| Output voltage | Survival(3) | –0.3 | 16 | V |
| $I_{OUT}$ (Survival) | | Short-circuit protected | | |
| Input-output voltage | Survival(4) | –0.3 | 16 | V |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$. The value $R_{\theta JA}$ for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 *Leadless Leadframe Package (LLP)* (SNOA401).. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2989 output must be diode-clamped to ground.
(4) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating junction temperature | –40 | 125 | °C |
| Operating input supply voltage | 2.1 | 16 | V |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LP2989 WSON (NGN) 8 PINS | LP2989 SOIC (D) 8 PINS | LP2989 VSSOP (DGK) 8 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance, High-K | 34.8 | 114.5 | 156.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 28.4 | 61.1 | 51.0 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.0 | 55.6 | 76.5 | |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | 9.7 | 4.9 | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 12.2 | 54.9 | 75.2 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.3 | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $V_{\overline{SD}}$ = 2 V.

| PARAMETER | | TEST CONDITIONS | LP2989AI-X.X(1) MIN | LP2989AI-X.X(1) TYP | LP2989AI-X.X(1) MAX | LP2989I-X.X(1) MIN | LP2989I-X.X(1) TYP | LP2989I-X.X(1) MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output voltage tolerance | | –0.75 | | 0.75 | –1.25 | | 1.25 | %$V_{NOM}$ |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V | –1.5 | | 1.5 | –2.5 | | 2.5 | |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | –4 | | 2.5 | –5 | | 3.5 | |
| | | 1 mA < $I_{OUT}$ < 500 mA, $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –25°C ≤ $T_J$ ≤ 125°C | –3.5 | | 2.5 | –4.5 | | 3.5 | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Output voltage line regulation | $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V | | 0.005 | 0.014 | | 0.005 | 0.014 | %/V |
| | | $V_{OUT(NOM)}$ + 1 V ≤ $V_{IN}$ ≤ 16 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.005 | 0.032 | | 0.005 | 0.032 | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | 1 mA < $I_{OUT}$ < 500 mA | | 0.4 | | | 0.4 | | %$V_{NOM}$ |
| $V_{IN} – V_{OUT}$ | Dropout voltage(2) | $I_{OUT}$ = 100 µA | | 1 | 3 | | 1 | 3 | mV |
| | | $I_{OUT}$ = 100 µA, –40°C ≤ $T_J$ ≤ 125°C | | 1 | 4 | | 1 | 4 | |
| | | $I_{OUT}$ = 200 mA | | 150 | 200 | | 150 | 200 | mV |
| | | $I_{OUT}$ = 200 mA, –40°C ≤ $T_J$ ≤ 125°C | | 150 | 300 | | 150 | 300 | |
| | | $I_{OUT}$ = 500 mA | | 310 | 425 | | 310 | 425 | mV |
| | | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ 125°C | | 310 | 650 | | 310 | 650 | |

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

## Electrical Characteristics (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ = 2 V.

| PARAMETER | | TEST CONDITIONS | LP2989AI-X.X(1) | | | LP2989I-X.X(1) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 100 µA | | 110 | 175 | | 110 | 175 | µA |
| | | $I_{OUT}$ = 100 µA, –40°C ≤ $T_J$ ≤ 125°C | | 110 | 200 | | 110 | 200 | |
| | | $I_{OUT}$= 200 mA | | 1 | 2 | | 1 | 2 | mA |
| | | $I_{OUT}$ = 200 mA, –40°C ≤ $T_J$ ≤ 125°C | | 1 | 3.5 | | 1 | 3.5 | |
| | | $I_{OUT}$ = 500 mA | | 3 | 6 | | 3 | 6 | mA |
| | | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ 125°C | | 3 | 9 | | 3 | 9 | |
| | | $\overline{SD}$ < 0.18 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 2 | | 0.5 | 2 | µA |
| | | $\overline{SD}$ < 0.4 V | | 0.05 | 0.8 | | 0.05 | 0.8 | |
| $I_{OUT(PK)}$ | Peak output current | $V_{OUT}$ ≥ $V_{OUT(NOM)}$ – 5% | 600 | 800 | | 600 | 800 | | mA |
| $I_{OUT(MAX)}$ | Short circuit current | $R_L$ = 0 (Steady State)(3) | | 1000 | | | 1000 | | mA |
| $e_n$ | Output noise voltage (RMS) | BW = 100 Hz to 100 kHz, $C_{OUT}$ = 10 µF, $C_{BYPASS}$ = .01 µF, $V_{OUT}$ = 2.5 V | | 18 | | | 18 | | $\mu V_{(RMS)}$ |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Ripple Rejection | f = 1 kHz, $C_{OUT}$ = 10 µF | | 60 | | | 60 | | dB |
| $\Delta V_{OUT}/\Delta T_D$ | Output voltage temperature coefficient | See(4), –40°C ≤ $T_J$ ≤ 125°C | | 20 | | | 20 | | ppm/°C |
| **$\overline{SHUTDOWN}$ INPUT** | | | | | | | | | |
| $V_{\overline{SD}}$ | $\overline{SD}$ Input voltage | $V_H$ = Output ON | | 1.4 | | | 1.4 | | V |
| | | $V_H$ = Output ON, –40°C ≤ $T_J$ ≤ 125°C | 1.6 | | | 1.6 | | | |
| | | $V_L$ = Output OFF | | 0.5 | | | 0.5 | | |
| | | $V_L$ = Output OFF, $I_{IN}$ ≤ 2 µA, –40°C ≤ $T_J$ ≤ 125°C | | | 0.18 | | | 0.18 | |
| $I_{\overline{SD}}$ | $\overline{SD}$ Input current | $\overline{SD}$ = 0 | | 0.001 | | | 0.001 | | µA |
| | | $\overline{SD}$ = 0, –40°C ≤ $T_J$ ≤ 125°C | | | –1 | | | –1 | |
| | | $\overline{SD}$ = 5 V | | 5 | | | 5 | | |
| | | $\overline{SD}$ = 5 V, –40°C ≤ $T_J$ ≤ 125°C | | | 15 | | | 15 | |
| **ERROR COMPARATOR** | | | | | | | | | |
| $I_{OH}$ | Output "HIGH" leakage | $V_{OH}$ = 16 V | | 0.001 | 1 | | 0.001 | 1 | µA |
| | | $V_{OH}$ = 16 V, –40°C ≤ $T_J$ ≤ 125°C | | 0.001 | 2 | | 0.001 | 2 | |
| $V_{OL}$ | Output "LOW" voltage | $V_{IN}$ = $V_{OUT(NOM)}$ – 0.5 V, $I_{OUT(COMP)}$ = 150 µA | | 150 | 220 | | 150 | 220 | mV |
| | | $V_{IN}$ = $V_{OUT(NOM)}$ – 0.5 V, $I_{OUT(COMP)}$ = 150 µA, –40°C ≤ $T_J$ ≤ 125°C | | 150 | 350 | | 150 | 350 | |
| $V_{THR(MAX)}$ | Upper threshold voltage | | –6 | –4.8 | –3.5 | –6 | –4.8 | –3.5 | $\%V_{OUT}$ |
| | | –40°C ≤ $T_J$ ≤ 125°C | –8.3 | –4.8 | –2.5 | –8.3 | –4.8 | –2.5 | |
| $V_{THR(MIN)}$ | Lower threshold voltage | | –8.9 | –6.6 | –4.9 | –8.9 | –6.6 | –4.9 | $\%V_{OUT}$ |
| | | –40°C ≤ $T_J$ ≤ 125°C | –13 | –6.6 | –3 | –13 | –6.6 | –3 | |
| HYST | Hysteresis | | | 2 | | | | | |

(3) See the *Typical Characteristics* section.
(4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

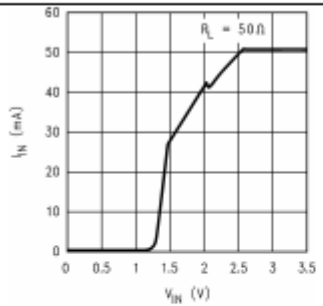



**Figure 7. Input Current vs $V_{IN}$**

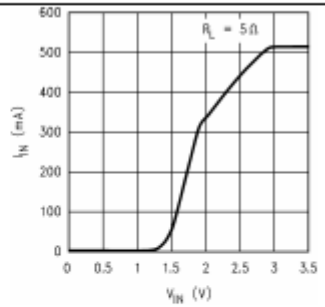



**Figure 8. Input Current vs $V_{IN}$**

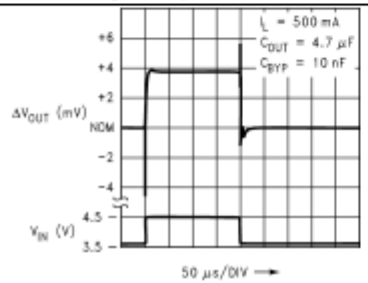



**Figure 9. Line Transient Response**

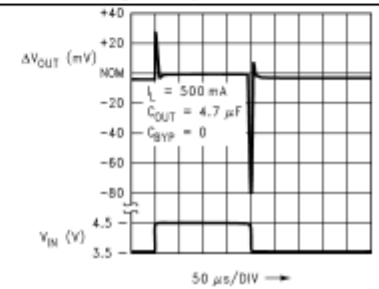



**Figure 10. Line Transient Response**

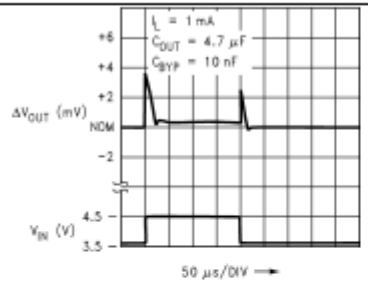



**Figure 11. Line Transient Response**

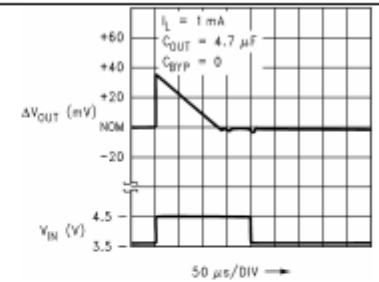



**Figure 12. Line Transient Response**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

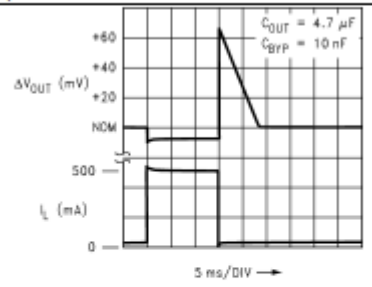



**Figure 13. Load Transient Response**

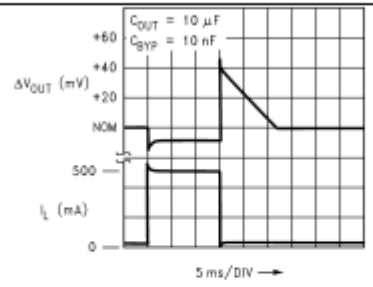



**Figure 14. Load Transient Response**

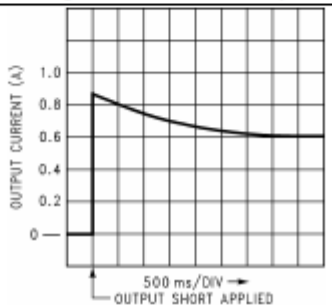



**Figure 15. Short Circuit Current**

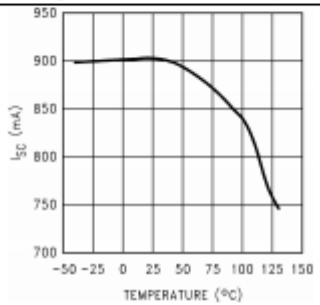



**Figure 16. Short Circuit Current vs Temperature**

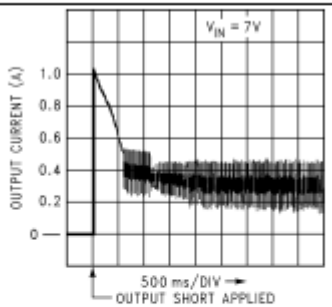



**Figure 17. Short Circuit Current**

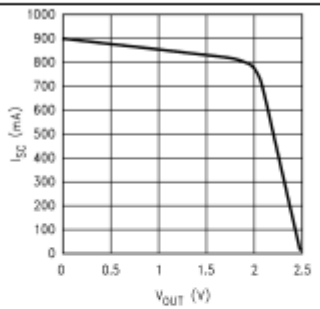



**Figure 18. Short Circuit Current vs $V_{OUT}$**


## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

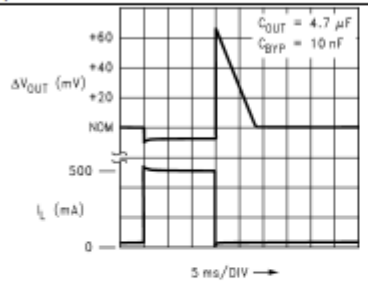




**Figure 13. Load Transient Response**

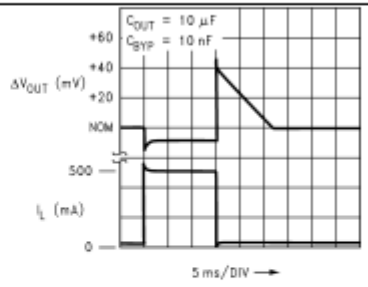



**Figure 14. Load Transient Response**

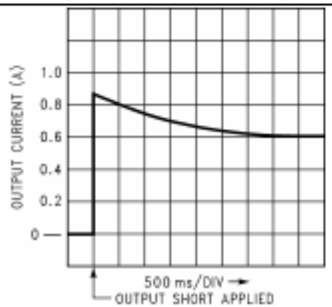



**Figure 15. Short Circuit Current**

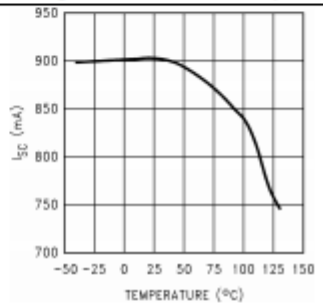



**Figure 16. Short Circuit Current vs Temperature**

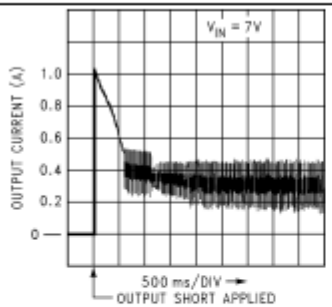



**Figure 17. Short Circuit Current**

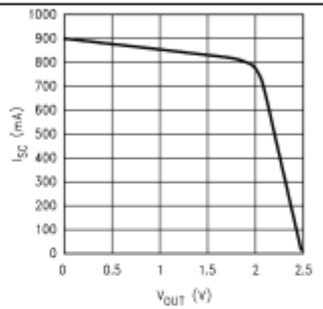



**Figure 18. Short Circuit Current vs $V_{OUT}$**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

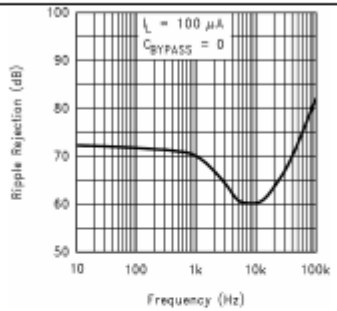



**Figure 19. Ripple Rejection**

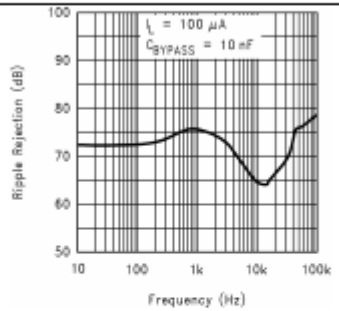



**Figure 20. Ripple Rejection**

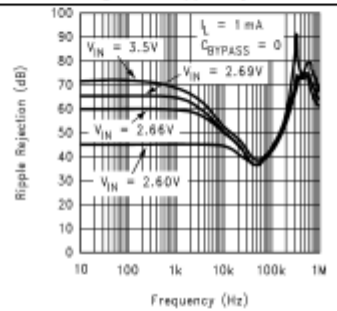



**Figure 21. Ripple Rejection**

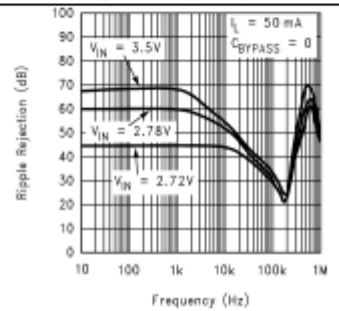



**Figure 22. Ripple Rejection**

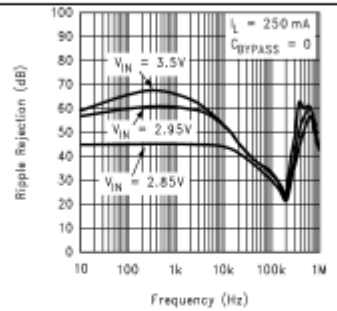



**Figure 23. Ripple Rejection**

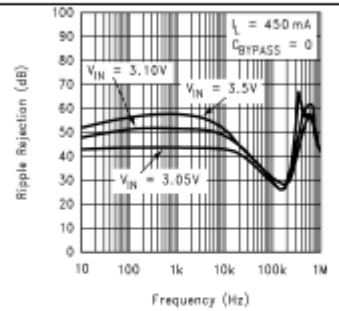



**Figure 24. Ripple Rejection**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

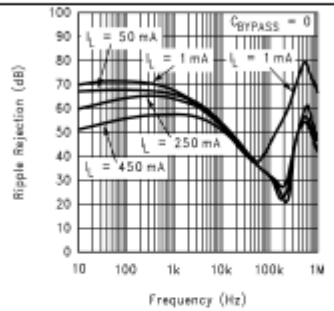



**Figure 25. Ripple Rejection**

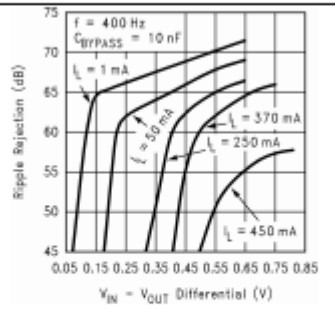



**Figure 26. Ripple Rejection in Dropout**

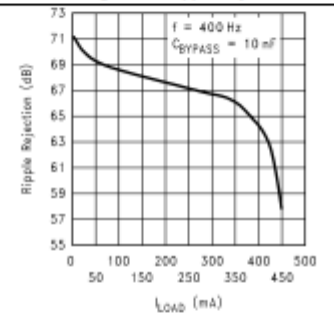



**Figure 27. Ripple Rejection vs Load**

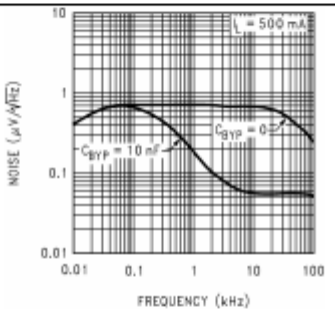



**Figure 28. Output Noise Density**

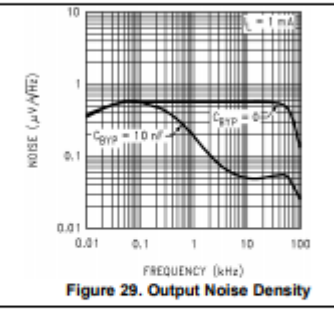



**Figure 29. Output Noise Density**

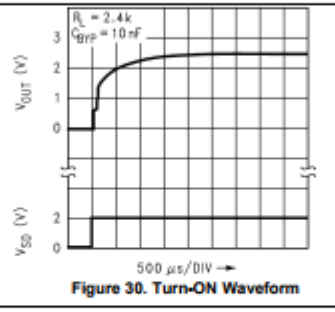



**Figure 30. Turn-ON Waveform**

## Typical Characteristics (continued)

$T_A$ = 25°C, $C_{OUT}$ = 4.7 µF, $C_{IN}$ = 2.2 µF, $\overline{SD}$ is tied to $V_{IN}$, $V_{IN}$ = $V_{OUT(NOM)}$+ 1 V, $I_{OUT}$ = 1 mA, $V_{OUT}$ = 2.5 V (unless otherwise specified)

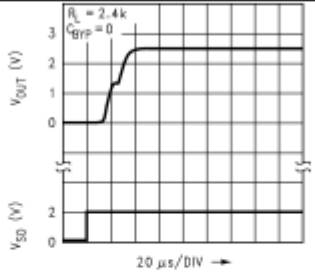



**Figure 31. Turn-ON Waveform**

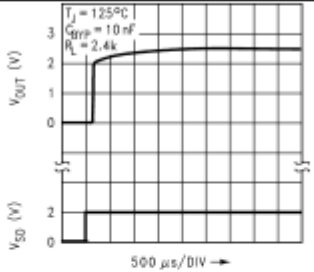



**Figure 32. Turn-ON Waveform**

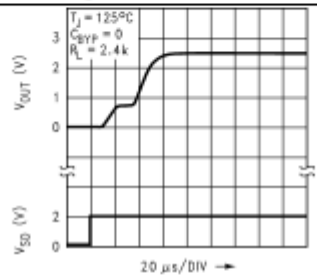



**Figure 33. Turn-ON Waveform**

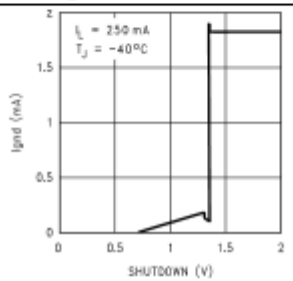



**Figure 34. $I_{GND}$ vs Shutdown**

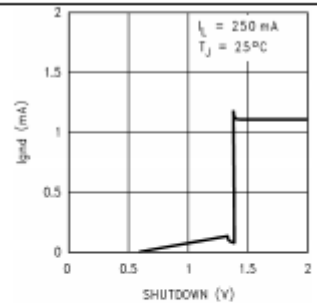



**Figure 35. $I_{GND}$ vs Shutdown**

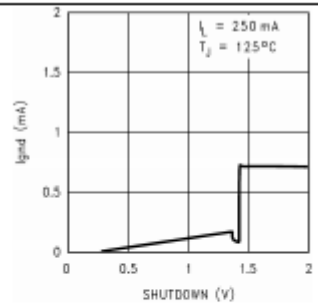



**Figure 36. $I_{GND}$ vs Shutdown**

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

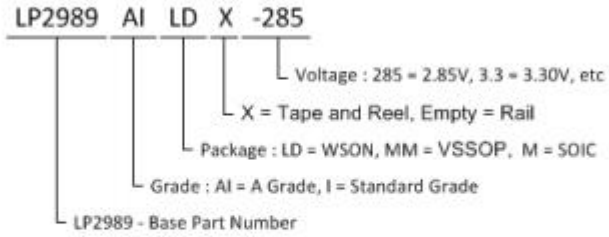



**Figure 45. POA Orderable Device Key**