16-Bit, 250 MSPS Analog-to-Digital Converter

Enhanced Product

AD9467-EP

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

FUNCTIONAL BLOCK DIAGRAM

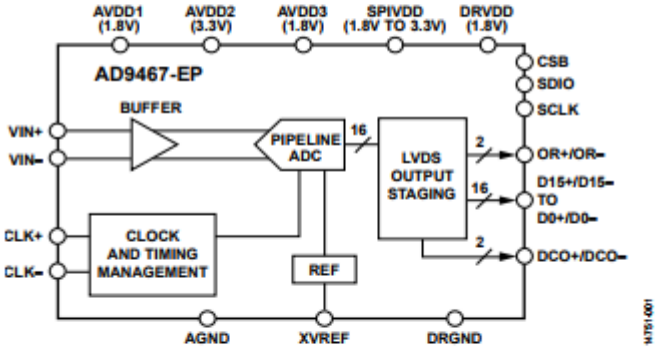

Figure 1.

ENHANCED PRODUCT FEATURES

- Extended temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- Qualification data available on request

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

GENERAL DESCRIPTION

The AD9467-EP is a 16-bit, monolithic, IF sampling analog-to-digital converter (ADC). It is optimized for high performance over wide bandwidths and ease of use. The product operates at a 250 MSPS conversion rate and is designed for wireless receivers, instrumentation, and test equipment that require a high dynamic range.

The ADC requires 1.8 V and 3.3 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are LVDS-compatible (ANSI-644-compatible) and include the means to reduce the overall current needed for short trace distances.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit. The internal power-down feature, when enabled via the serial port interface (SPI), typically consumes less than 5 mW.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467-EP is available in a Pb-free, 72-lead, LFCSP specified over the −55°C to +125°C extended temperature range.

Additional application and technical information can be found in the AD9467 data sheet.

PRODUCT HIGHLIGHTS

1. IF optimization capability used to improve SFDR.
2. Outstanding SFDR performance for IF sampling applications such as multicarrier, multimode 3G, and 4G cellular base station receivers.
3. Ease of use: on-chip reference, high input impedance buffer, adjustable analog input range, and an output clock to simplify data capture.
4. Packaged in a Pb-free, 72-lead LFCSP package.
5. Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of input clock pulse widths.
6. Standard SPI supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding).

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

Parameter[1]	Temp	Min	Typ	Max	Unit
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS at 2.5 V p-p FS					
f_{IN1} = 70 MHz, f_{IN2} = 72 MHz	25°C		97		dBFS
f_{IN1} = 170 MHz, f_{IN2} = 172 MHz	25°C		91		dBFS

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		0.8		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		2.5		pF
LOGIC INPUTS (SCLK, CSB, SDIO)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.7/3.1		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.3	V
DIGITAL OUTPUTS (D0+ to D15+, D0− to D15−, DCO+, DCO−, OR+, OR−)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		545	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This depends on if SPIVDD is tied to a 1.8 V or 3.3 V supply.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 4.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate	Full	50		250	MSPS
Clock Pulse Width High (t_{CH})	Full		2		ns
Clock Pulse Width Low (t_{CL})	Full		2		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	25°C		3		ns
Rise Time (t_R) (20% to 80%)	25°C		200		ps
Fall Time (t_F) (20% to 80%)	25°C		200		ps
DCO Propagation Delay (t_{CPD})	25°C		3		ns
DCO to Data Delay (t_{SKEW})	Full	−200		+200	ps
Wake-Up Time (Power-Down)	Full		100		ms
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1.2		ns
Aperture Uncertainty (Jitter)	25°C		60		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR-4 material.

Timing Diagrams

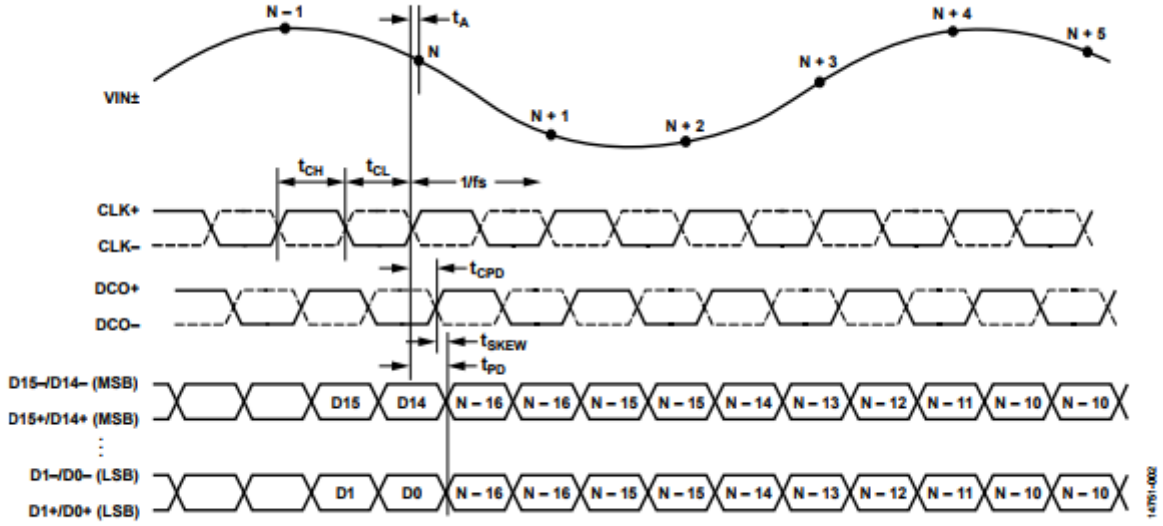

Figure 2. 16-Bit Output Data Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
Electrical		
AVDD1, AVDD3	AGND	−0.3 V to +2.0 V
AVDD2, SPIVDD	AGND	−0.3 V to +3.9 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD2, SPIVDD	AVDD1, AVDD3	−2.0 V to +3.9 V
AVDD1, AVDD3	DRVDD	−2.0 V to +2.0 V
AVDD2, SPIVDD	DRVDD	−2.0 V to +3.9 V
Digital Outputs (Dx+, Dx−, OR+, OR−, DCO+, DCO−)	DRGND	−0.3 V to DRVDD + 0.2 V
CLK+, CLK−	AGND	−0.3 V to AVDD1 + 0.2 V
VIN+, VIN−	AGND	−0.3 V to +3.6 V
XVREF	AGND	−0.3 V to AVDD1 + 0.2 V
SCLK, CSB, SDIO	AGND	−0.3 V to SPIVDD + 0.2 V
Environmental		
Operating Temperature Range (Ambient)		−55°C to +125°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JB}[1, 3, 4]	θ_{JC}[1, 5]	Unit
0.0	15.7°C/W	7.5°C/W	0.5°	°C/W
1.0	13.7°C/W	N/A	N/A	°C/W
2.5	12.3°C/W	N/A	N/A	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A means not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

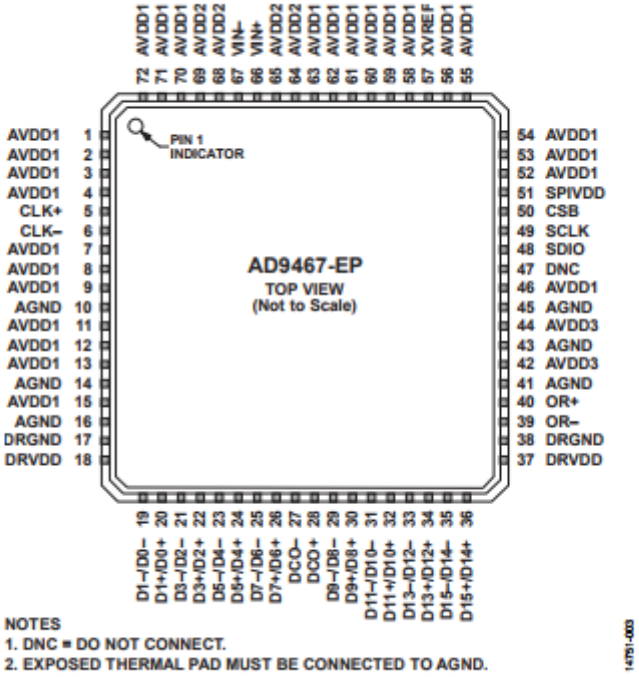

Figure 3. Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Paddle. The exposed paddle must be connected to AGND.
10, 14, 16, 41, 43, 45	AGND	Analog Ground.
1, 2, 3, 4, 7, 8, 9, 11, 12, 13, 15, 46, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 63, 70, 71, 72	AVDD1	1.8 V Analog Supply.
64, 65, 68, 69	AVDD2	3.3 V Analog Supply.
42, 44	AVDD3	1.8 V Analog Supply.
51	SPIVDD	1.8 V or 3.3 V SPI Supply
17, 38	DRGND	Digital Output Driver Ground.
18, 37	DRVDD	1.8 V Digital Output Driver Supply.
67	VIN–	Analog Input Complement.
66	VIN+	Analog Input True.
6	CLK–	Clock Input Complement.
5	CLK+	Clock Input True.
19	D1–/D0–	D1 and D0 (LSB) Digital Output Complement.
20	D1+/D0+	D1 and D0 (LSB) Digital Output True.
21	D3–/D2–	D3 and D2 Digital Output Complement.
22	D3+/D2+	D3 and D2 Digital Output True.
23	D5–/D4–	D5 and D4 Digital Output Complement.
24	D5+/D4+	D5 and D4 Digital Output True.
25	D7–/D6–	D7 and D6 Digital Output Complement.
26	D7+/D6+	D7 and D6 Digital Output True.
29	D9–/D8–	D9 and D8 Digital Output Complement.
30	D9+/D8+	D9 and D8 Digital Output True.
31	D11–/D10–	D11 and D10 Digital Output Complement.
32	D11+/D10+	D11 and D10 Digital Output True.
33	D13–/D12–	D13 and D12 Digital Output Complement.
34	D13+/D12+	D13 and D12 Digital Output True.
35	D15–/D14–	D15 (MSB) and D14 Digital Output Complement.

Pin No.	Mnemonic	Description
36	D15+/D14+	D15 (MSB) and D14 Digital Output True.
27	DCO−	Data Clock Digital Output Complement.
28	DCO+	Data Clock Digital Output True.
39	OR−	Out-of-Range Digital Output Complement.
40	OR+	Out-of-Range Digital Output True.
47	DNC	Do Not Connect (Leave Pin Floating).
48	SDIO	Serial Data Input/Output.
49	SCLK	Serial Clock.
50	CSB	Chip Select Bar.
57	XVREF	External VREF Option.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted, buffer current optimized for best SFDR performance.

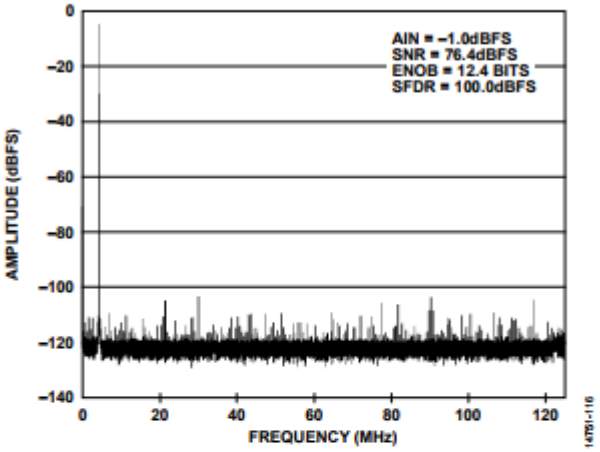

Figure 4. Single-Tone FFT with f_{IN} = 4.3 MHz, 2.5 V p-p FS

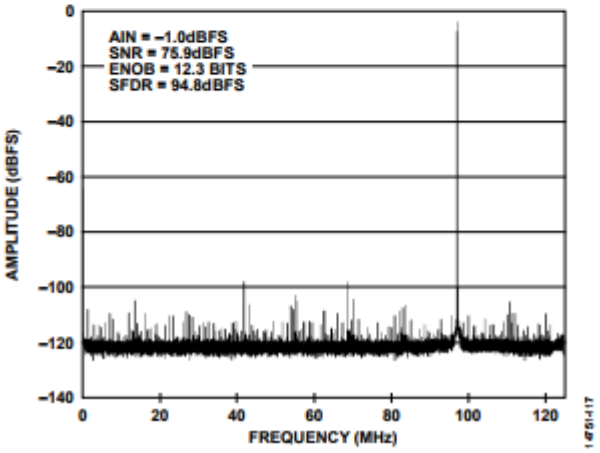

Figure 5. Single-Tone FFT with f_{IN} = 97.3 MHz, 2.5 V p-p FS

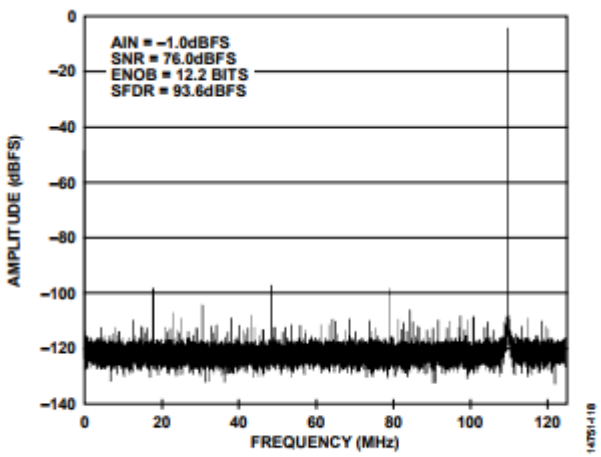

Figure 6. Single-Tone FFT with f_{IN} = 140.3 MHz, 2.5 V p-p FS

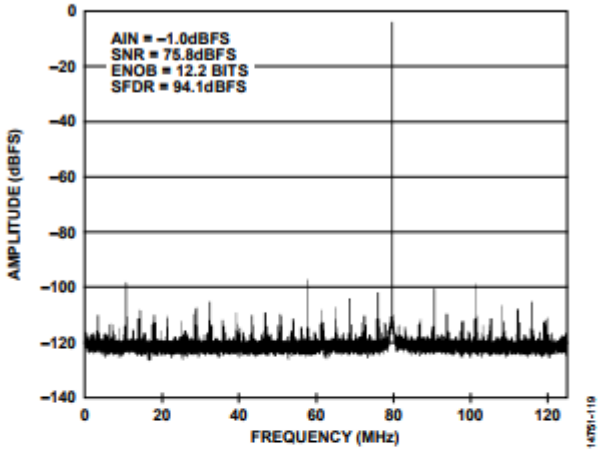

Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz, 2.5 V p-p FS

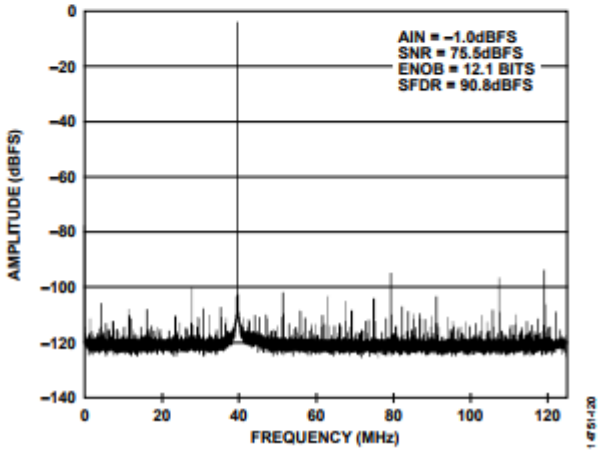

Figure 8. Single-Tone FFT with f_{IN} = 210.3 MHz, 2.5 V p-p FS

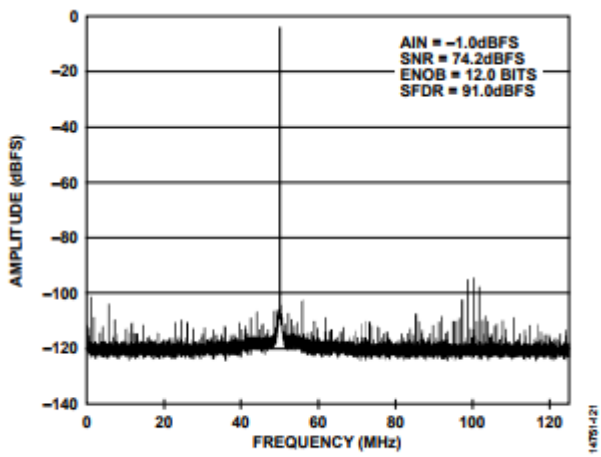

Figure 9. Single-Tone FFT with f_{IN} = 300.3 MHz, 2.5 V p-p FS

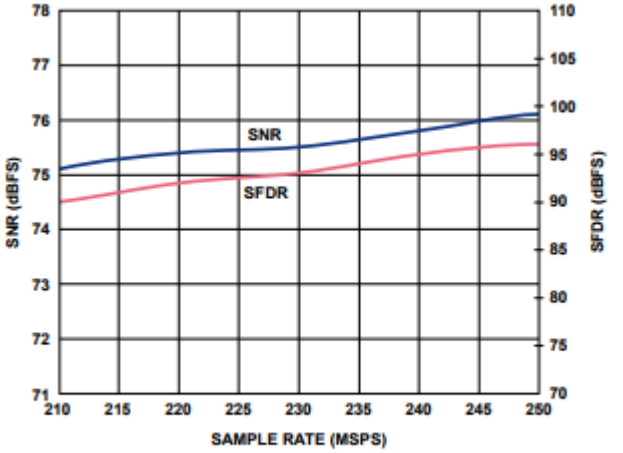

Figure 10. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 97.3 MHz, 2.5 V p-p FS

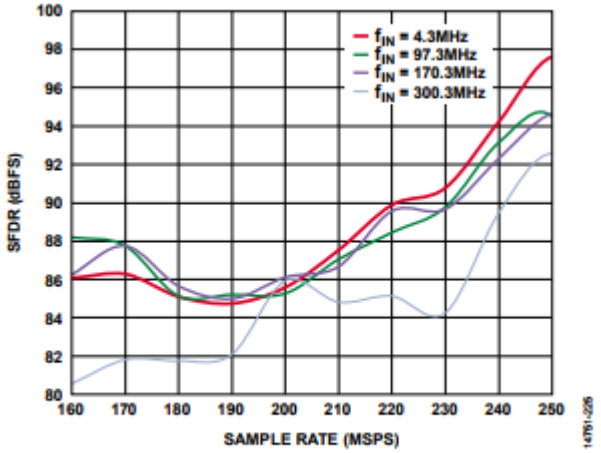

Figure 11. SFDR vs. f_{SAMPLE}, 2.5 V p-p FS

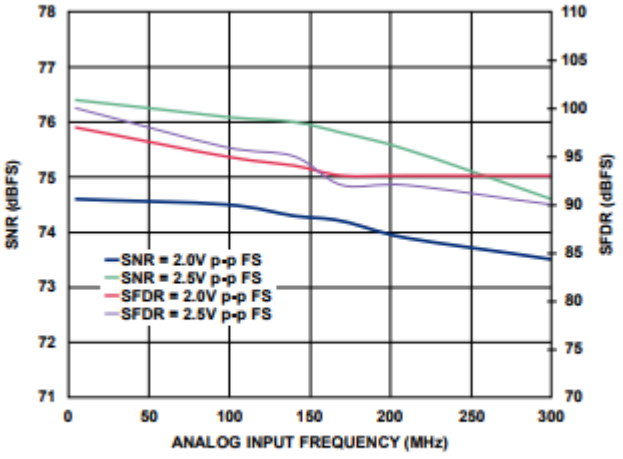

Figure 12. SNR/SFDR vs. f_{IN}, 2.0/2.5 V p-p FS

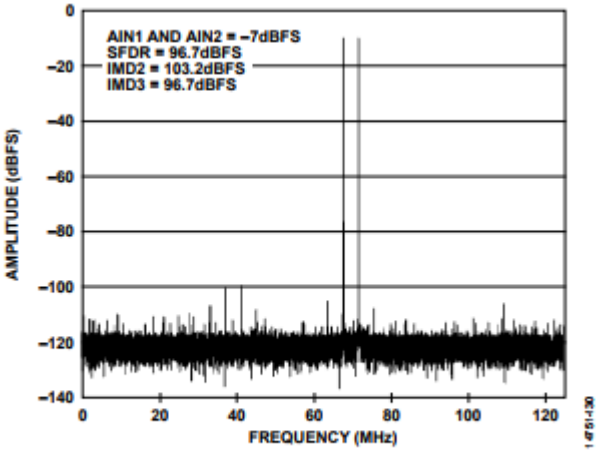

Figure 13. Two-Tone FFT with f_{IN1} = 70 MHz and f_{IN2} = 72 MHz, 2.5 V p-p FS

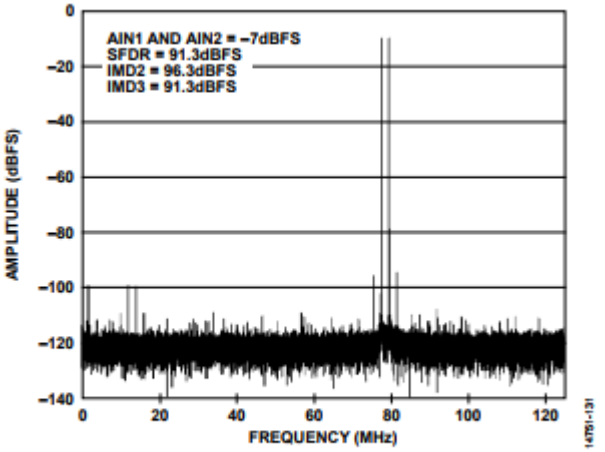

Figure 14. Two-Tone FFT with f_{IN1} = 170 MHz and f_{IN2} = 172 MHz, 2.5 V p-p FS

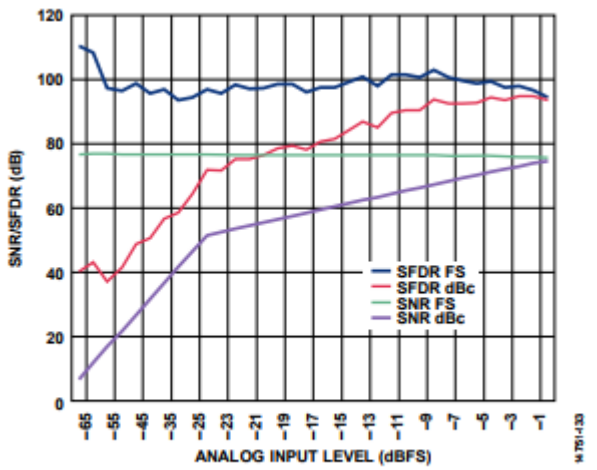

Figure 15. SNR/SFDR vs. Analog Input Level, f_{IN} = 97.3 MHz, 2.5 V p-p FS,

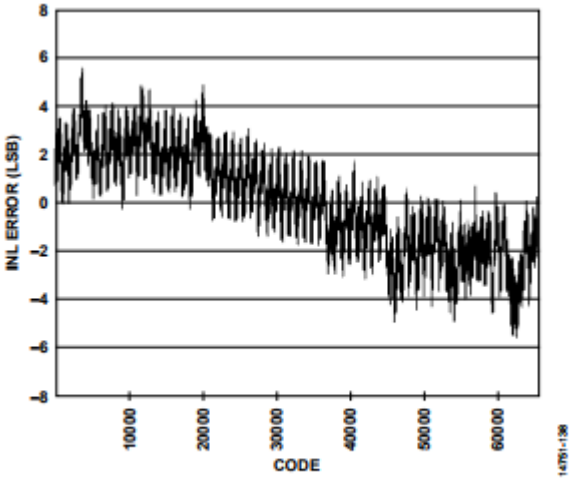

Figure 16. INL, f_{IN} = 4.3 MHz, 2.5 V p-p FS

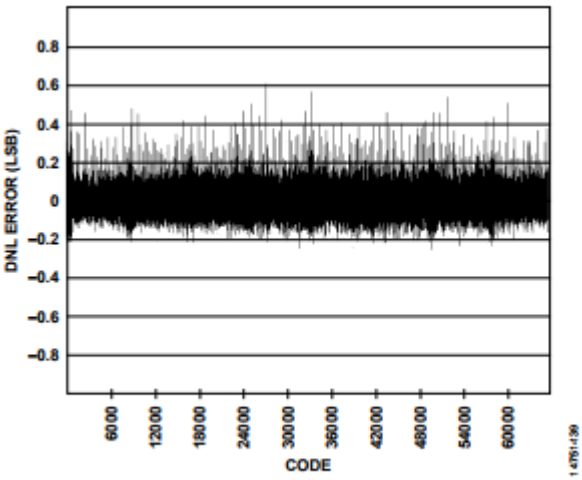

Figure 17. DNL, f_{IN} = 4.3 MHz, 2.5 V p-p FS

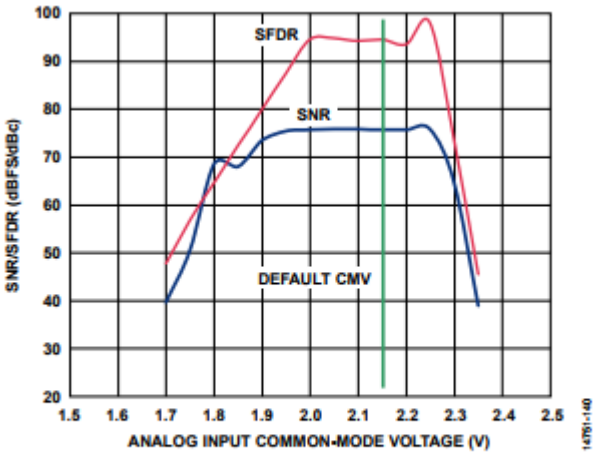

Figure 18. SNR/SFDR vs. Analog Input Common-Mode Voltage, AIN = 100 MHz, 2.5 V p-p FS

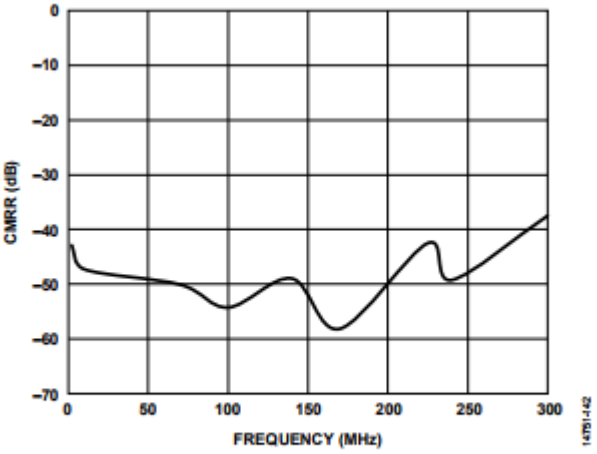

Figure 19. Common-Mode Rejection Ratio (CMRR)

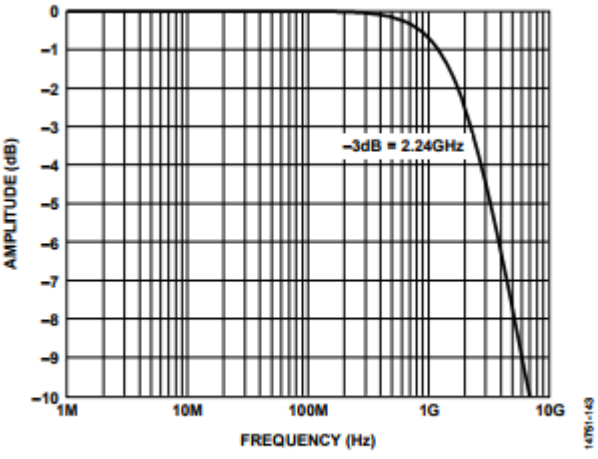

Figure 20. Converter AC Bandwidth

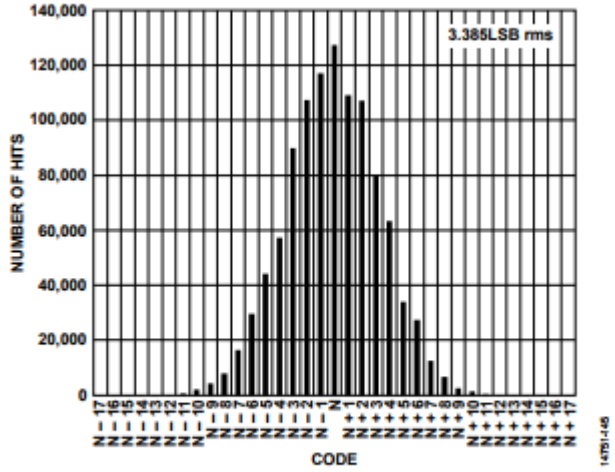

Figure 21. Input-Referred Noise Histogram, 2.5 V p-p FS

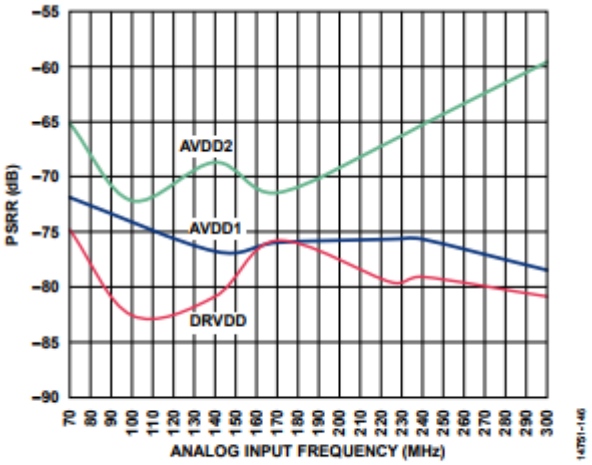

Figure 22. Power Supply Rejection (PSR)

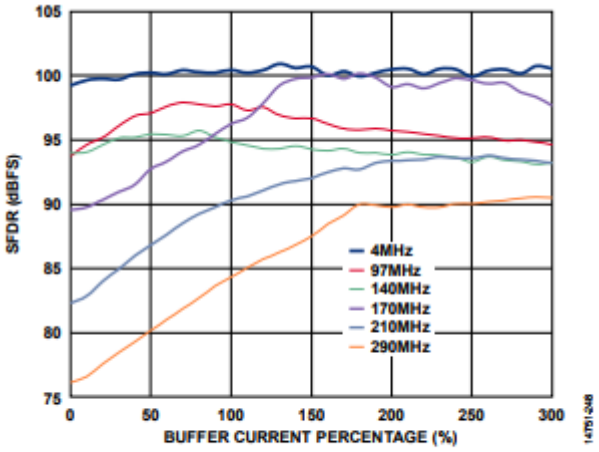

Figure 23. SFDR Performance vs. Buffer Current Percentage Over Analog Input Frequency

OUTLINE DIMENSIONS

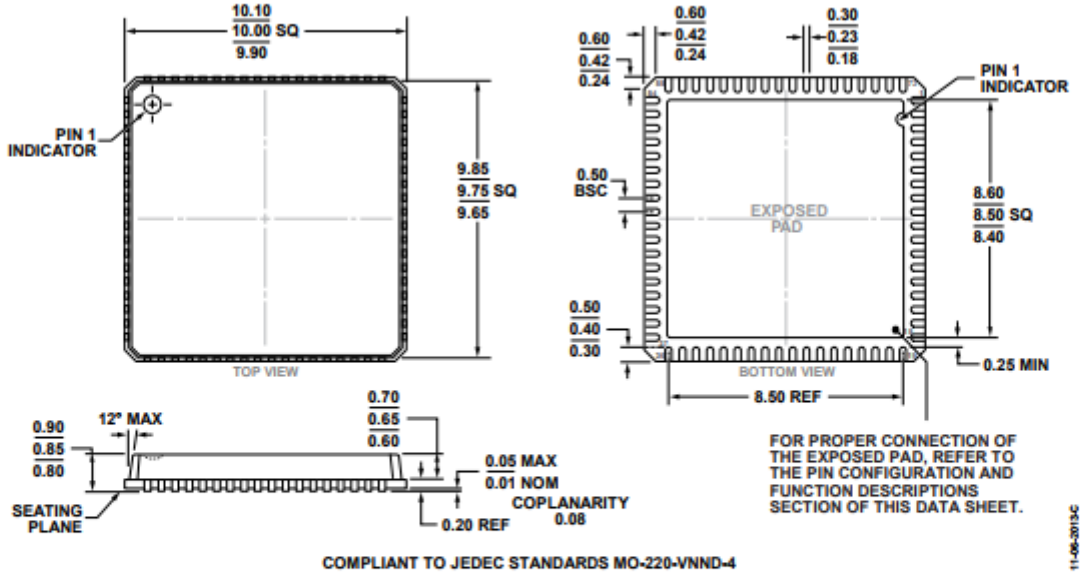

Figure 24. 72-Lead Lead Frame Chip Scale Package, Exposed Pad [LFCSP]
10 mm × 10 mm Body and 0.85 mm Package Height
(CP-72-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9467SCPZ-250-EP	−55°C to +125°C	72-Lead LFCSP	CP-72-5
AD9467SCPZ250EPRL7	−55°C to +125°C	72-Lead LFCSP	CP-72-5