12-Bit, 170/210 MSPS 3.3 V A/D Converter

AD9430

FEATURES

- SNR = 65 dB @ f_{IN} = 70 MHz @ 210 MSPS
- ENOB of 10.6 @ f_{IN} = 70 MHz @ 210 MSPS (−0.5 dBFS)
- SFDR = 80 dBc @ f_{IN} = 70 MHz @ 210 MSPS (−0.5 dBFS)
- Excellent linearity:
  - DNL = ±0.3 LSB (typical)
  - INL = ±0.5 LSB (typical)
- 2 output data options:
  - Demultiplexed 3.3 V CMOS outputs each @ 105 MSPS
  - Interleaved or parallel data output option
- LVDS at 210 MSPS
- 700 MHz full-power analog bandwidth
- On-chip reference and track-and-hold
- Power dissipation = 1.3 W typical @ 210 MSPS
- 1.5 V input voltage range
- 3.3 V supply operation
- Output data format option
- Data sync input and data clock output provided
- Clock duty cycle stabilizer

GENERAL DESCRIPTION

The AD9430 is a 12-bit, monolithic, sampling analog-to-digital converter (ADC) optimized for high performance, low power, and ease of use. The product operates up to a 210 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution.

The ADC requires a 3.3 V power supply and a differential ENCODE clock for full performance operation. The digital outputs are TTL/CMOS or LVDS compatible and support either twos complement or offset binary format. Separate output power supply pins support interfacing with 3.3 V CMOS logic.

Two output buses support demultiplexed data up to 105 MSPS rates in CMOS mode. A data sync input is supported for proper output data port alignment in CMOS mode, and a data clock output is available for proper output data timing. In LVDS mode, the chip provides data at the ENCODE clock rate.

Fabricated on an advanced BiCMOS process, the AD9430 is available in a 100-lead, surface-mount plastic package (100 e-PAD TQFP) specified over the industrial temperature range (−40°C to +85°C).

FUNCTIONAL BLOCK DIAGRAM

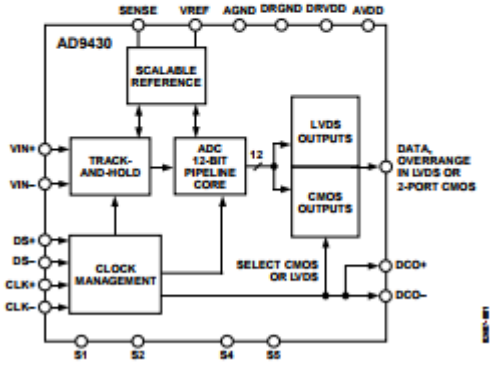

Figure 1.

APPLICATIONS

- Wireless and wired broadband communications
- Cable reverse path
- Communications test equipment
- Radar and satellite subsystems
- Power amplifier linearization

PRODUCT HIGHLIGHTS

1. High performance.
   Maintains 65 dB SNR @ 210 MSPS with a 65 MHz input.
2. Low power.
   Consumes only 1.3 W @ 210 MSPS.
3. Ease of use.
   LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample-and-hold provide flexibility in system design. Use of a single 3.3 V supply simplifies system power supply design.
4. Out of range (OR) feature.
   The OR output bit indicates when the input signal is beyond the selected input range.
5. Pin compatible with 10-bit AD9411 (LVDS only).

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DC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −0.5 dBFS, internal reference, full scale = 1.536 V, LVDS output mode, unless otherwise noted.

Table 1.

			AD9430-170			AD9430-210			
Parameter	Temp	Test Level	Min	Typ	Max	Min	Typ	Max	Unit
RESOLUTION				12					Bits
ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	25°C	I	−3		+3	−3		+3	mV
Gain Error	25°C	I	−5		+5	−5		+5	% FS
Differential Nonlinearity (DNL)	25°C	I	−1	± 0.3	+1	−1	± 0.3	+1	LSB
	Full	VI	−1	± 0.3	+1.5	−1	± 0.3	+1.5	LSB
Integral Nonlinearity (INL)	25°C	I	−1.5	± 0.5	+1.5	−1.75	± 0.3	+1.75	LSB
	Full	VI	−2.25	± 0.5	+2.25	−2.5	± 0.3	+2.5	LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		58			58		µV/°C
Gain Error	Full	V		0.02			0.02		%/°C
Reference Out (VREF)	Full	V		+0.12/−0.24			+0.12/−0.24		mV/°C
REFERENCE									
Reference Out (VREF)	25°C	I	1.15	1.235	1.3	1.15	1.235	1.3	V
Output Current[1]	25°C	IV			3.0			3.0	mA
I_{VREF} Input Current[2]	25°C	I			20			20	µA
I_{SENSE} Input Current[2]	25°C	I		1.6	5.0		1.6	5.0	mA
ANALOG INPUTS (VIN+, VIN−)[3]									
Differential Input Voltage Range (S5 = GND)	Full	V		1.536			1.536		V
Differential Input Voltage Range (S5 = AVDD)	Full	V		0.766			0.766		V
Input Common-Mode Voltage	Full	VI	2.65	2.8	2.9	2.65	2.8	2.9	V
Input Resistance	Full	VI	2.2	3	3.8	2.2	3	3.8	kΩ
Input Capacitance	25°C	V		5			5		pF
POWER SUPPLY (LVDS Mode)									
AVDD	Full	IV	3.1	3.3	3.6	3.2	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents									
I_{ANALOG} (AVDD = 3.3 V)[4]	Full	VI		335	372		390	450	mA
$I_{DIGITAL}$ (DRVDD = 3.3 V)[4]	Full	VI		55	62		55	62	mA
Power Dissipation[4]	Full	VI		1.29	1.43		1.5	1.7	W
Power Supply Rejection	25°C	V		−7.5			−7.5		mV/V

Parameter	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
POWER SUPPLY (CMOS Mode)									
AVDD	Full	IV	3.1	3.3	3.6	3.2	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents									
I_{AVDD} (AVDD = 3.3 V)[5]	Full	IV		335	372		390	450	mA
I_{DRVDD} (DRVDD = 3.3 V)[5]	Full	IV		24	30		30	30	mA
Power Dissipation[5]	Full	IV		1.1			1.3		W
Power Supply Rejection	25°C	V		−7.5			−7.5		mV/V

[1] Internal reference mode; SENSE = Floats.
[2] External reference mode; SENSE = DRVDD, VREF driven by external 1.23 V reference.
[3] SS (Pin 1) = GND. See the Analog Input section. SS = GND in all dc and ac tests, unless otherwise noted.
[4] I_{AVDD} and I_{DRVDD} are measured with an analog input of 10.3 MHz, −0.5 dBFS, sine wave, rated ENCODE rate, and in LVDS output mode. See Typical Performance Characteristics and Application Notes sections for I_{DRVDD}. Power consumption is measured with a dc input at rated ENCODE rate in LVDS output mode.
[5] I_{AVDD} and I_{DRVDD} are measured with an analog input of 10.3 MHz, −0.5 dBFS, sine wave, rated ENCODE rate, and in CMOS output mode. See Typical Performance Characteristics and Application Notes sections for I_{DRVDD}. Power consumption is measured with a dc input at rated ENCODE rate in CMOS output mode.

AD9430

AC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −0.5 dBFS, internal reference, full scale = 1.536 V, LVDS output mode, unless otherwise noted.[1]

Table 2.

Parameter		Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
SNR										
Analog Input @ −0.5 dBFS	10 MHz	25°C	I	63.5	65		62.5	64.5		dB
	70 MHz	25°C	I	63	65		62.5	64.5		dB
	100 MHz	25°C	V		65			64.5		dB
	240 MHz	25°C	V		61			61		dB
SINAD										
Analog Input @ −0.5 dBFS	10 MHz	25°C	I	63.5	65		62.5	64.5		dB
	70 MHz	25°C	I	63	65		62.5	64.5		dB
	100 MHz	25°C	V		65			64.5		dB
	240 MHz	25°C	V		60			60		dB
EFFECTIVE NUMBER OF BITS (ENOB)										
	10 MHz	25°C	I	10.3	10.6		10.2	10.5		Bits
	70 MHz	25°C	I	10.3	10.6		10.2	10.5		Bits
	100 MHz	25°C	V		10.6			10.5		Bits
	240 MHz	25°C	V		9.8			9.8		Bits
WORST HARMONIC (2nd or 3rd)										
Analog Input @ −0.5 dBFS, 10 MHz	10 MHz	25°C	I		−85	−75		−84	−74	dBc
	70 MHz	25°C	I		−85	−75		−84	−74	dBc
	100 MHz	25°C	V		−77			−77		dBc
	240 MHz	25°C	V		−63			−63		dBc
WORST HARMONIC (4th or Higher)										
Analog Input @ −0.5 dBFS, 10 MHz	10 MHz	25°C	I		−87	−78		−87	−77	dBc
	70 MHz	25°C	I		−87	−78		−87	−77	dBc
	100 MHz	25°C	V		−77			−77		dBc
	240 MHz	25°C	V		−63			−63		dBc
TWO-TONE IMD[2]										
F1, F2 @ −7 dBFS		25°C	V		−75			−75		dBc
ANALOG INPUT BANDWIDTH		25°C	V		700			700		MHz

[1] All ac specifications tested by differentially driving CLK+ and CLK−.
[2] F1 = 28.3 MHz, F2 = 29.3 MHz.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
ENCODE AND DS INPUTS (CLK+, CLK−, DS+, DS−)[1]									
Differential Input Voltage[2]	Full	IV	0.2			0.2			V
Common-Mode Voltage[3]	Full	VI	1.375	1.5	1.575	1.375	1.5	1.575	V
Input Resistance	Full	VI	3.2	5.5	6.5	3.2	5.5	6.5	kΩ
Input Capacitance	25°C	V		4			4		pF
LOGIC INPUTS (S1, S2, S4, S5)									
Logic 1 Voltage	Full	IV	2.0			2.0			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
Logic 1 Input Current	Full	VI			190			190	µA
Logic 0 Input Current	Full	VI			10			10	µA
Input Resistance	25°C	V		30			30		kΩ
Input Capacitance	25°C	V		4			4		pF
LOGIC OUTPUTS (CMOS Mode)									
Logic 1 Voltage[4]	Full	IV	DRVDD −0.05			DRVDD −0.05			V
Logic 0 Voltage[4]	Full	IV			0.05			0.05	V
LOGIC OUTPUTS (LVDS Mode)[4, 5]									
V_{OD} Differential Output Voltage	Full	VI	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	VI	1.125		1.375	1.125		1.375	V
Output Coding			Twos complement or binary			Twos complement or binary			

[1] ENCODE (Clock) and DS inputs identical on the chip. See the Equivalent Circuits section.
[2] All ac specifications tested by driving CLK+ and CLK− differentially. |(CLK+) − (CLK−)| > 200 mV.
[3] ENCODE (Clock) inputs' common-mode can be externally set, such that 0.9 V < (CLK+ or CLK−) < 2.6 V.
[4] Digital output logic levels: DRVDD = 3.3 V, C_{LOAD} = 5 pF.
[5] LVDS R_{TERM} = 100 Ω, LVDS output current set resistor (R_{SET}) = 3.74 kΩ (1% tolerance).

AD9430

SWITCHING SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 4.

Parameter (Conditions)	Temp	Test Level	AD9430-170 Min	AD9430-170 Typ	AD9430-170 Max	AD9430-210 Min	AD9430-210 Typ	AD9430-210 Max	Unit
Maximum Conversion Rate[1]	Full	VI	170			210			MSPS
Minimum Conversion Rate[1]	Full	V			40			40	MSPS
CLK+ Pulse Width High (t_{EH})[1]	Full	IV	2		12.5	2		12.5	ns
CLK+ Pulse Width Low (t_{EL})[1]	Full	IV	2		12.5	2		12.5	ns
DS Input Setup Time (t_{SDS})[2]	Full	IV	−0.5			−0.5			ns
DS Input Hold Time (t_{HDS})[2]	Full	IV	1.75			1.75			ns
OUTPUT (CMOS Mode)									
Valid Time (t_V)	Full	IV	2			2			ns
Propagation Delay (t_{PD})	Full	IV		3.8	5		3.8	5	ns
Rise Time (t_R) (20% to 80%)	25°C	V		1			1		ns
Fall Time (t_F) (20% to 80%)	25°C	V		1			1		ns
DCO Propagation Delay (t_{CPD})	Full	IV		3.8	5		3.8	5	ns
Data to DCO Skew (t_{PD} to t_{CPD})	Full	IV	−0.5	0	+0.5	−0.5	0	+0.5	ns
Interleaved Mode (A, B Latency)	Full	IV		14, 14			14, 14		Cycles
Parallel Mode (A, B Latency)	Full	IV		15, 14			15, 14		Cycles
OUTPUT (LVDS Mode)									
Valid Time (t_V)	Full	VI	2.0			2.0			ns
Propagation Delay (t_{PD})	Full	VI		3.2	4.3		3.2	4.3	ns
Rise Time (t_R) (20% to 80%)	25°C	V		0.5			0.5		ns
Fall Time (t_F) (20% to 80%)	25°C	V		0.5			0.5		ns
DCO Propagation Delay (t_{CPD})	Full	VI	1.8	2.7	3.8	1.8	2.7	3.8	ns
Data to DCO Skew (t_{PD} − t_{CPD})	Full	IV	0.2	0.5	0.8	0.2	0.5	0.8	ns
Latency	Full	IV		14			14		Cycles
APERTURE DELAY (t_A)	25°C	V		1.2			1.2		ns
APERTURE UNCERTAINTY (Jitter, t_J)	25°C	V		0.25			0.25		ps rms
OUT OF RANGE RECOVERY TIME (CMOS and LVDS)	25°C	V			1			1	Cycles

[1] All ac specifications tested by differentially driving CLK+ and CLK−.
[2] DS inputs used in CMOS mode only.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DRVDD	4 V
Analog Inputs	−0.5 V to AVDD + 0.5 V
Digital Inputs	−0.5 V to DRVDD + 0.5 V
REFIN Inputs	−0.5 V to AVDD + 0.5 V
Digital Output Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
θ_{JA}[1]	25°C/W, 32°C/W

[1] Typical θ_{JA} = 32°C/W (heat slug not soldered); typical θ_{JA} = 25°C/W (heat slug soldered) for multilayer board in still air with solid ground plane.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Table 6.

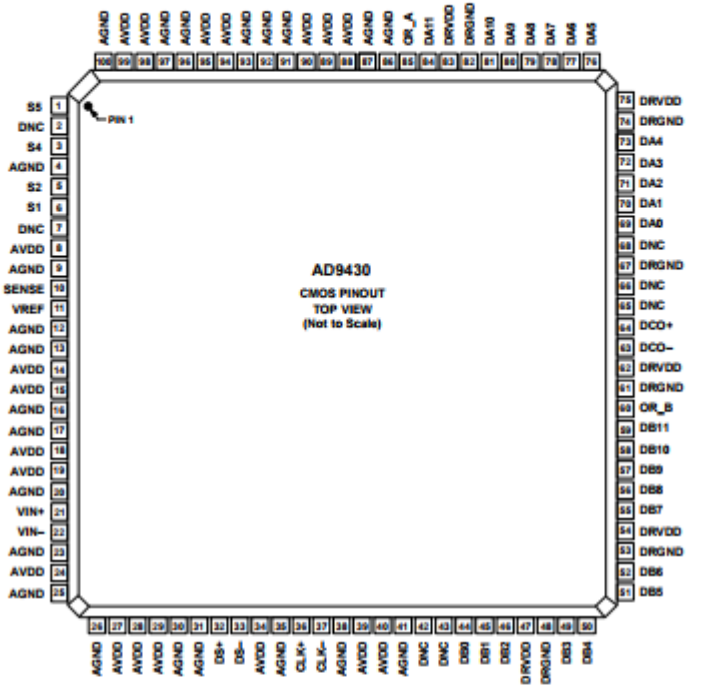
Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD9430

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE AD9430 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

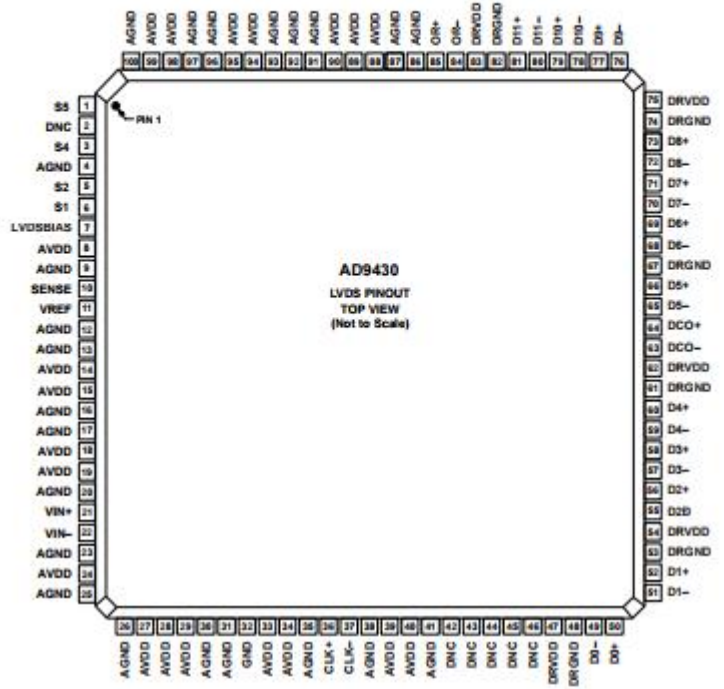
Figure 4. CMOS Dual-Mode Pin Configuration

Table 7. CMOS Mode Pin Function Descriptions

Pin Number	Mnemonic	Description
1	S5	Full-Scale Adjust Pin. AVDD sets f_S = 0.768 V p-p differential, GND sets f_S = 1.536 V p-p differential.
2, 7, 42, 43, 65, 66, 68	DNC	Do Not Connect.
3	S4	Interleaved, Parallel Select Pin. High = interleaved.
4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100	AGND[1]	Analog Ground.
5	S2	Output Mode Select. Low = dual-port CMOS, high = LVDS.
6	S1	Data Format Select. Low = binary, high = twos complement for both CMOS and LVDS modes.
8, 14, 15, 18, 19, 24, 27, 28, 29, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99	AVDD	3.3 V Analog Supply.
10	SENSE	Reference Mode Select Pin. Float for internal reference operation.
11	VREF	1.235 V Reference I/O—Function Dependent on SENSE.
21	VIN+	Analog Input—True.
22	VIN–	Analog Input—Complement.
32	DS+	Data Sync (Input)—True. Tie low if not used.
33	DS–[2]	Data Sync (Input)—Complement. Tie high if not used.

Pin Number	Mnemonic	Description
36	CLK+	Clock Input—True.
37	CLK–	Clock Input—Complement.
44	DB0	B Port Output Data Bit (LSB).
45	DB1	B Port Output Data Bit.
46	DB2	B Port Output Data Bit.
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
48, 53, 61, 67, 74, 82	DRGND[1]	Digital Output Ground.
49	DB3	B Port Output Data Bit.
50	DB4	B Port Output Data Bit.
51	DB5	B Port Output Data Bit.
52	DB6	B Port Output Data Bit.
55	DB7	B Port Output Data Bit.
56	DB8	B Port Output Data Bit.
57	DB9	B Port Output Data Bit.
58	DB10	B Port Output Data Bit.
59	DB11	B Port Output Data Bit (MSB).
60	OR_B	B Port Overrange.
63	DCO–	Data Clock Output—Complement.
64	DCO+	Data Clock Output—True.
69	DA0	A Port Output Data Bit (LSB).
70	DA1	A Port Output Data Bit.
71	DA2	A Port Output Data Bit.
72	DA3	A Port Output Data Bit.
73	DA4	A Port Output Data Bit.
76	DA5	A Port Output Data Bit.
77	DA6	A Port Output Data Bit.
78	DA7	A Port Output Data Bit.
79	DA8	A Port Output Data Bit.
80	DA9	A Port Output Data Bit.
81	DA10	A Port Output Data Bit.
84	DA11	A Port Output Data Bit (MSB).
85	OR_A	A Port Overrange.

[1] AGND and DRGND should be tied together to a common ground plane.
[2] DS Complement (DS–); can be tied to AVDD (as recommended) or left floating with no ill effects.



NOTES
1. THE AD9430 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

Figure 5. LVDS Mode Pin Configuration

Table 8. LVDS Mode Pin Function Descriptions

Pin Number	Mnemonic	Description
1	S5	Full-Scale Adjust Pin. AVDD sets f_S = 0.768 V p-p differential, GND sets f_S = 1.536 V p-p differential.
2, 42 to 46	DNC	Do Not Connect.
3	S4	Control Pin for CMOS Mode. Tie low when operating in LVDS mode.
4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100	AGND[1]	Analog Ground.
5	S2	Output Mode Select. GND = dual-port CMOS; AVDD = LVDS.
6	S1	Data Format Select. GND = binary, AVDD = twos complement.
7	LVDSBIAS	Set Pin for LVDS Output Current. Place 3.74 kW resistor terminated to ground.
8, 14, 15, 18, 19, 24, 27, 28, 29, 33, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99	AVDD[2]	3.3 V Analog Supply.
10	SENSE	Reference Mode Select Pin. Float for internal reference operation.
11	VREF	1.235 V Reference I/O—Function Dependent on SENSE.
21	VIN+	Analog Input—True.

Pin Number	Mnemonic	Description
22	VIN–	Analog Input—Complement.
32	GND	Data Sync (Input)—Not Used in LVDS Mode. Tie to GND.
36	CLK+	Clock Input—True (LVPECL Levels).
37	CLK–	Clock Input—Complement (LVPECL Levels).
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
48, 53, 61, 67, 74, 82	DRGND[1]	Digital Output Ground.
49	D0–	D0 Complement Output Bit (LSB).
50	D0+	D0 True Output Bit (LSB).
51	D1–	D1 Complement Output Bit.
52	D1+	D1 True Output Bit.
55	D2–	D2 Complement Output Bit.
56	D2+	D2 True Output Bit.
57	D3–	D3 Complement Output Bit.
58	D3+	D3 True Output Bit.
59	D4–	D4 Complement Output Bit.
60	D4+	D4 True Output Bit.
63	DCO–	Data Clock Output—Complement.
64	DCO+	Data Clock Output—True.
65	D5–	D5 Complement Output Bit.
66	D5+	D5 True Output Bit.
68	D6–	D6 Complement Output Bit.
69	D6+	D6 True Output Bit.
70	D7–	D7 Complement Output Bit.
71	D7+	D7 True Output Bit.
72	D8–	D8 Complement Output Bit.
73	D8+	D8 True Output Bit.
76	D9–	D9 Complement Output Bit.
77	D9+	D9 True Output Bit.
78	D10–	D10 Complement Output Bit.
79	D10+	D10 True Output Bit.
80	D11–	D11 Complement Output Bit.
81	D11+	D11 True Output Bit.
84	OR–	Overrange Complement Output Bit.
85	OR+	Overrange True Output Bit.

[1] AGND and DRGND should be tied together to a common ground plane.
[2] Pin 33 can be tied to AVDD (as recommended) or left floating with no ill effects