LT1394

7ns, Low Power, Single Supply, Ground-Sensing Comparator

FEATURES

- **UltraFast™: 7ns**
- **Low Power: 6mA**
- **Low Offset Voltage: 0.8mV**
- Operates Off Single 5V or Dual ±5V Supplies
- Input Common Mode Extends to Negative Supply
- No Minimum Input Slew Rate Requirement
- Complementary TTL Outputs
- Inputs Can Exceed Supplies without Phase Reversal
- Pin Compatible with LT1016, LT1116 and LT1671
- Output Latch Capability
- Available in 8-Lead MSOP and SO Packages

APPLICATIONS

- High Speed A/D Converters
- Zero-Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V/F Coverters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

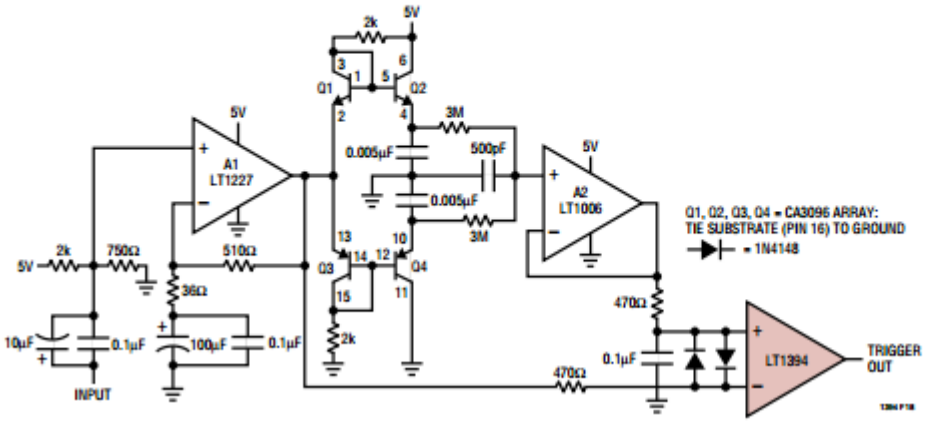
The LT®1394 is an UltraFast (7ns) comparator with complementary outputs and latch. The input common mode range extends from 1.5V below the positive supply down to the negative supply rail. Like the LT1016, LT1116 and LT1671, this comparator has complementary outputs designed to interface directly to TTL or CMOS logic. The LT1394 may operate from either a single 5V supply or dual ±5V supplies. Low offset voltage specifications and high gain allow the LT1394 to be used in precision applications.

The LT1394 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL, CMOS or passive loads with minimal cross-conduction current. Unlike other fast comparators, the LT1394 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

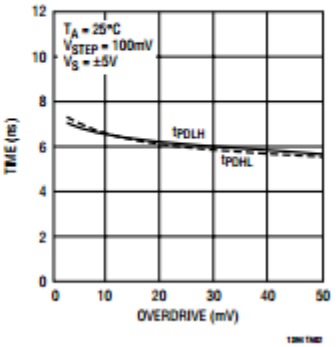
The LT1394 has an internal, TTL/CMOS compatible latch for retaining data at the outputs. The latch holds data as long as the LATCH pin is held high. Device parameters such as gain, offset and negative power supply current are not significantly affected by variations in negative supply voltage.

TYPICAL APPLICATION

45MHz Single Supply Adaptive Trigger



Propagation Delay vs Input Overdrive

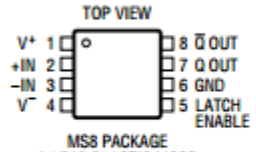


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12V
Positive Supply Voltage 7V
Negative Supply Voltage ..... –7V
Differential Input Voltage ..... ±12V
Input and Latch Current (Note 2) ..... ±10mA
Output Current (Continuous)(Note 2) ..... ±20mA

Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 3) ... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

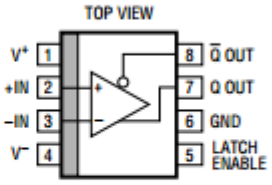
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LT1394CMS8
MS8 PART MARKING
LTBH



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1394CS8 LT1394IS8
S8 PART MARKING
1394 1394I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 4)			0.8	2.5	mV
			●			4.0	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		4		µV/°C
I_{OS}	Input Offset Current				0.1	0.5	µA
			●			0.8	µA
I_B	Input Bias Current	(Note 5)			2	4.5	µA
			●			7.0	µA
V_{CMR}	Input Voltage Range (Note 6)		●	–5		3.5	V
		Single 5V Supply	●	0		3.5	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 3.5V$, $T_A > 0°C$		55	100		dB
		$-5V \le V_{CM} \le 3.3V$, $T_A \le 0°C$		55			dB
		Single 5V Supply					
		$0V \le V_{CM} \le 3.5V$, $T_A > 0°C$		55	100		dB
		$0V \le V_{CM} \le 3.3V$, $T_A \le 0°C$		55			dB
PSRR	Power Supply Rejection Ratio	$4.6V \le V^+ \le 5.4V$	●	50	65		dB
		$-7V \le V^- \le -2V$	●	65	100		dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		750	1600		V/V
V_{OH}	Output Voltage Swing High	$V^+ \ge 4.6V$, I_{OUT} = 1mA	●	2.7	3.1		V
		$V^+ \ge 4.6V$, I_{OUT} = 4mA	●	2.4	3.0		V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing Low	I_{OUT} = –4mA I_{OUT} = –10mA	● ●		0.3 0.4	0.5	V V
I^+	Positive Supply Current		 ●		6	8.5 10.0	mA mA
I^-	Negative Supply Current		 ●		1.2	2.2 2.5	mA mA
V_{IH}	LATCH Pin High Input Voltage		●	2			V
V_{IL}	LATCH Pin Low Input Voltage		●			0.8	V
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V	●		–4	–10	µA
t_{PD}	Propagation Delay (Note 7)	ΔV_{IN} = 100mV, V_{OD} = 5mV	 ●		7	9 14	ns ns
Δt_{PD}	Differential Propagation Delay (Note 7)	ΔV_{IN} = 100mV, V_{OD} = 5mV			0.5	2.2	ns
t_{LPD}	Latch Propagation Delay (Note 8)				6		ns
t_{SU}	Latch Setup Time (Note 8)				–0.4		ns
t_H	Latch Hold Time (Note 8)				2		ns
$t_{PW(D)}$	Minimum Disable Pulse Width				3		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified perforamnce through design and characterization. It has not been tested.

Note 3: The LT1394CMS8 and LT1394CS8 are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. The LT1394IS8 is guaranteed to meet the extended temperature limits.

Note 4: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V.

Note 5: Input bias current (I_B) is defined as the average of the two input currents.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization.

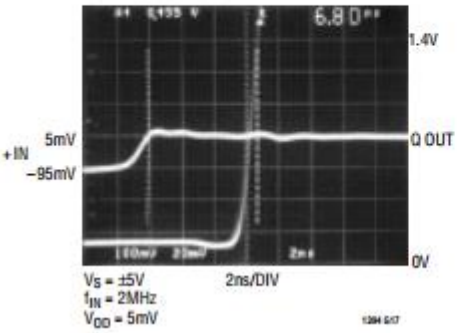
Note 7: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1394 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS}. Differential propagation delay is defined as:

$$\Delta t_{PD} = t_{PDLH} - t_{PDHL}$$

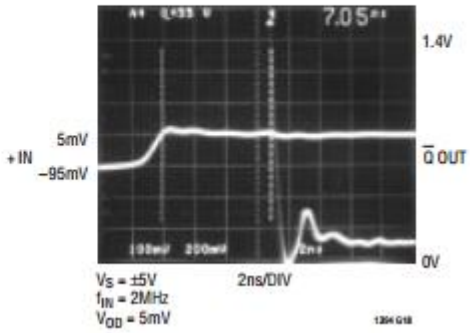
Note 8: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the LATCH pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable.

TYPICAL PERFORMANCE CHARACTERISTICS

t_{PD}^+ Response Time to 5mV Overdrive



t_{PD}^- Response Time to 5mV Overdrive



PIN FUNCTIONS

V^+ (Pin 1): Positive Supply Voltage. Normally 5V.

+IN (Pin 2): Noninverting Input.

–IN (Pin 3): Inverting Input.

V^- (Pin 4): Negative Supply Voltage. Normally either 0V or –5V.

LATCH ENABLE (Pin 5): Latch Control Pin. When high, the outputs remain in a latched condition, independent of the current state of the inputs.

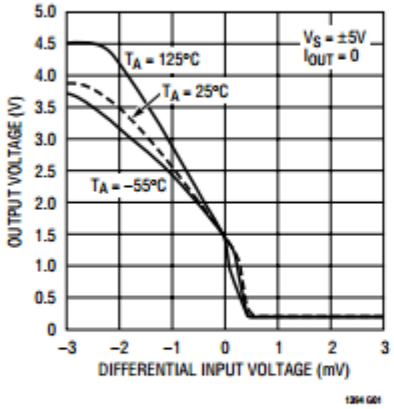
GND (Pin 6): Ground.

Q OUT (Pin 7): Noninverting Logic Output. This pin is high when +IN is above –IN and LATCH ENABLE is low.

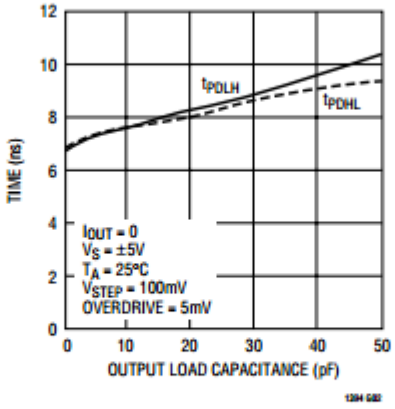
$\overline{Q}$ OUT (Pin 8): Inverting Logic Output. This pin is low when +IN is above –IN and LATCH ENABLE is low.

TYPICAL PERFORMANCE CHARACTERISTICS

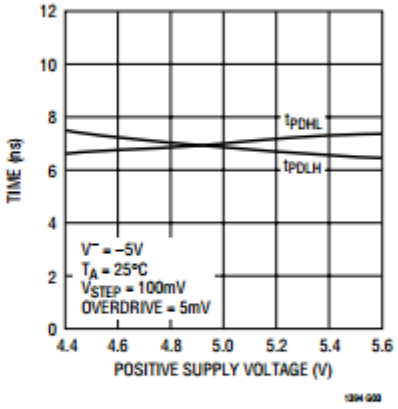
Gain Characteristics



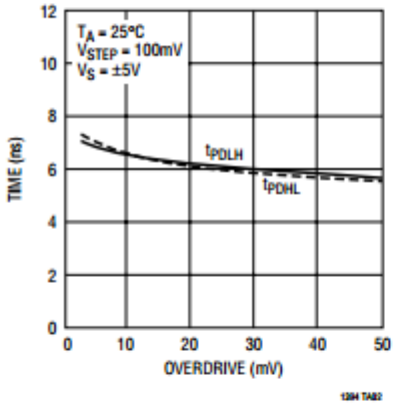
Propagation Delay vs Load Capacitance



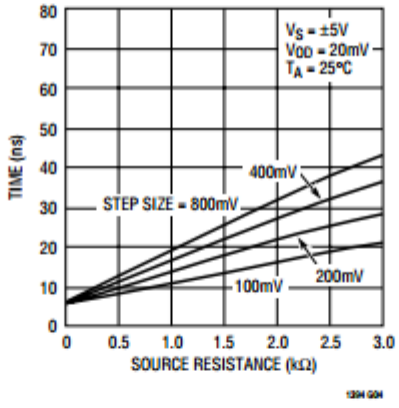
Propagation Delay vs Positive Supply Voltage



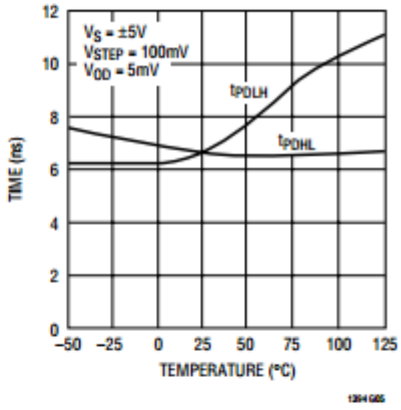
Propagation Delay vs Input Overdrive



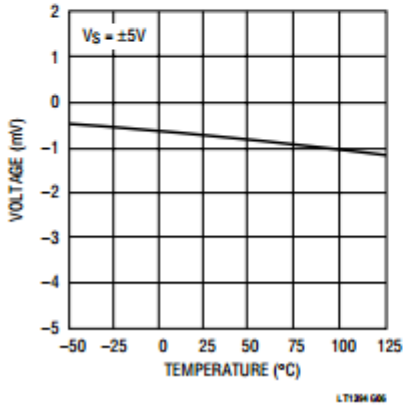
Propagation Delay vs Source Resistance



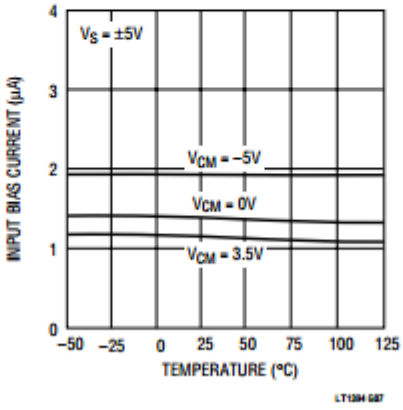
Propagation Delay vs Temperature



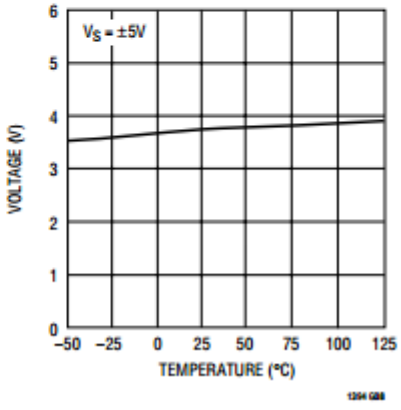
Input Offset Voltage vs Temperature



Input Bias Current vs Temperature



Positive Common Mode Limit vs Temperature



TIMING DIAGRAMS