150 MSPS, Wideband, Digital Downconverter (DDC)

AD6636

FEATURES

- 4/6 independent wideband processing channels
- Processes 6 wideband carriers (UMTS, CDMA2000)
- 4 single-ended or 2 LVDS parallel input ports (16 linear bit plus 3-bit exponent) running at 150 MHz
- Supports 300 MSPS input using external interface logic
- Three 16-bit parallel output ports operating up to 200 MHz
- Real or complex input ports
- Quadrature correction and dc correction for complex inputs
- Supports output rate up to 34 MSPS per channel
- RMS/peak power monitoring of input ports
- Programmable attenuator control for external gain ranging
- 3 programmable coefficient FIR filters per channel
- 2 decimating half-band filters per channel
- 6 programmable digital AGC loops with 96 dB range
- Synchronous serial I/O operation (SPI®-, SPORT-compatible)
- Supports 8-bit or 16-bit microport modes
- 3.3 V I/O, 1.8 V CMOS core
- User-configurable, built-in, self-test (BIST) capability
- JTAG boundary scan

APPLICATIONS

- Multicarrier, multimode digital receivers
- GSM, EDGE, PHS, UMTS, WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Micro and pico cell systems, software radios
- Broadband data applications
- Instrumentation and test equipment
- Wireless local loops
- In-building wireless telephony

FUNCTIONAL BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM

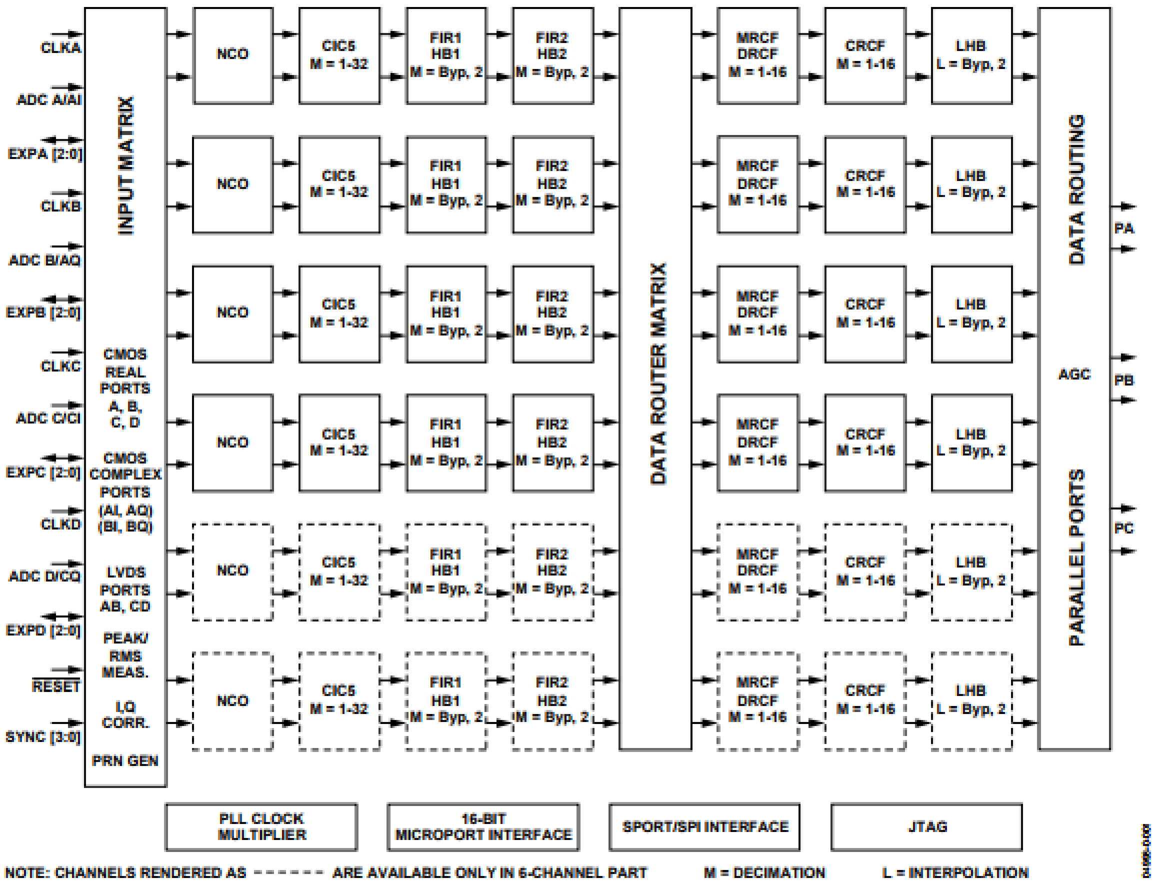


Figure 1.

GENERAL DESCRIPTION

The AD6636 is a digital downconverter intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals. The AD6636 has been optimized for the demanding filtering requirements of wideband standards, such as CDMA2000, UMTS, and TD-SCDMA, but is flexible enough to support wider standards such as WiMAX. The AD6636 is designed for radio systems that use either an IF sampling ADC or a baseband sampling ADC.

The AD6636 channels have the following signal processing stages: a frequency translator, a fifth-order cascaded integrated comb filter, two sets of cascaded fixed-coefficient FIR and half-band filters, three cascaded programmable coefficient sum-of-product FIR filters, an interpolating half-band filter (IHB), and a digital automatic gain control (AGC) block. Multiple modes are supported for clocking data into and out of the chip and provide flexibility for interfacing to a wide variety of digitizers. Programming and control are accomplished via serial or microport interfaces.

Input ports can take input data at up to 150 MSPS. Up to 300 MSPS input data can be supported using two input ports (some external interface logic is required) and two internal channels processing in tandem. Biphase filtering in the output data router is selected to complete the combined filtering mode. The four input ports can operate in CMOS mode, or two ports can be combined for LVDS input mode. The maximum input data rate for each input port is 150 MHz.

Frequency translation is accomplished with a 32-bit complex numerically controlled oscillator (NCO). It has greater than 110 dBc SFDR. This stage translates either a real or complex input signal from intermediate frequency (IF) to a baseband complex digital output. Phase and amplitude dither can be enabled on-chip to improve spurious performance of the NCO. A 16-bit phase-offset word is available to create a known phase relationship between multiple AD6636 chips or channels. The NCO can also be bypassed so that baseband I and Q inputs can be provided directly from baseband sampling ADCs through input ports.

Following frequency translation is a fifth-order CIC filter with a programmable decimation between 1 and 32. This filter is used to lower the sample rate efficiently, while providing sufficient alias rejection at frequencies with higher frequency offsets from the signal of interest.

Following the CIC5 are two sets of filters. Each set has a non-decimating FIR filter and a decimate-by-2 half-band filter. The FIR1 filter provides about 30 dB of rejection, while the HB1 filter provides about 77 dB of rejection. They can be used together to achieve a 107 dB stop band alias rejection, or they can be individually bypassed to save power. The FIR2 filter provides about 30 dB of rejection, while the HB2 filter provides about 65 dB of rejection. The filters can be used either together to achieve more than 95 dB stop band alias rejection, or can be individually bypassed to save power. FIR1 and HB1 filters can run with a maximum input rate of 150 MSPS. In contrast, FIR2 and HB2 can run with a maximum input rate of 75 MSPS (input rate to FIR2 and HB2 filters).

The programmable filtering is divided into three cascaded RAM coefficient filters (RCFs) for flexible and power efficient filtering. The first filter in the cascade is the MRCF, consisting of a programmable nondecimating FIR. It is followed by programmable FIR filters (DRCF) with decimation from 1 to 16. They can be used either together to provide high rejection filters, or independently to save power. The maximum input rate to the MRCF is one-fourth of the PLL clock rate.

The channel RCF (CRCF) is the last programmable FIR filter with programmable decimation from 1 to 16. It typically is used to meet the spectral mask requirements for the air standard of interest. This could be an RRC, antialiasing filter or any other real data filter. Decimation in preceding blocks is used to keep the input rate of this stage as low as possible for the best filter performance.

The last filter stage in the chain is an interpolate-by-2 half-band filter, which is used to up-sample the CRCF output to produce higher output oversampling. Signal rejection requirements for this stage are relaxed because preceding filters have filtered the blockers and adjacent carriers already.

Each input port of the AD6636 has its own clock used for latching onto the input data, but the Input Port A clock (CLKA) is also used as the input for an on-board PLL clock multiplier. The output of the PLL clock is used for processing all filters and processing blocks beyond the data router following the CIC filter. The PLL clock can be programmed to have a maximum clock rate of 200 MHz.

A data routing block (DR) is used to distribute data from the CICs to the various channel filters. This block allows multiple back-end filter chains to work together to process high bandwidth signals or to make even sharper filter transitions than a single channel can perform. It can also allow complex filtering operations to be achieved in the programmable filters.

The digital AGC provides the user with scaled digital outputs based on the rms level of the signal present at the output of the digital filters. The user can set the requested level and time constant of the AGC loop for optimum performance of the postprocessor. This is a critical function in the base station for CDMA applications where the power level must be well controlled going into the RAKE receivers. It has programmable clipping and rounding control to provide different output resolutions.

The overall filter response for the AD6636 is the composite of all the combined filter stages. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage minimizes overall power consumption. Data from the device is interfaced to a DSP/FPGA/baseband processor via either high speed parallel ports (preferred) or a DSP-compatible microprocessor interface.

The AD6636 is available both in 4-channel and 6-channel versions. The data sheet primarily discusses the 6-channel part. The only difference between the 6-channel and 4-channel devices is that Channel 4 and Channel 5 are not available on the 4-channel version, (see Figure 1). The 4-channel device still has the same input ports, output ports, and memory map. The memory map section for Channel 4 and Channel 5 can be programmed and read back, but it serves no purpose.

PRODUCT HIGHLIGHTS

- Six independent digital filtering channels
- 101 dB SNR noise performance, 110 dB spurious performance
- Four input ports capable of 150 MSPS input data rates
- RMS/peak power monitoring of input ports and 96 dB range AGCs before the output ports
- Three programmable RAM coefficient filters, three half-band filters, two fixed coefficient filters, and one fifth-order CIC filter per channel
- Complex filtering and biphase filtering (300 MSPS ADC input) by combining filtering capability of multiple channels
- Three 16-bit parallel output ports operating at up to a 200 MHz clock
- Black*fin*®-compatible and *Tiger*SHARC®-compatible 16-bit microprocessor port
- Synchronous serial communications port is compatible with most serial interface standards, SPORT, SPI, and SSR

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
VDDCORE	Full	IV	1.7	1.8	1.9	V
VDDIO	Full	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$	Full	IV	−40	+25	+85	°C

ELECTRICAL CHARACTERISTICS[1]

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS (NOT 5 V TOLERANT)						
Logic Compatibility	Full	IV	3.3			V CMOS
Logic 1 Voltage	Full	IV	2.0		3.6	V
Logic 0 Voltage	Full	IV	−0.3		+0.8	V
Logic 1 Current	Full	IV		1	10	μA
Logic 0 Current	Full	IV		1	10	μA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV	3.3			V CMOS
Logic 1 Voltage (I_{OH} = 0.25 mA)	Full	IV	2.0	VDDIO − 0.2		V
Logic 0 Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
SUPPLY CURRENTS						
WCDMA (61.44 MHz) Example[1]						
$I_{VDDCORE}$	25°C	V		450		mA
I_{VDDIO}	25°C	V		50		mA
CDMA 2000 (61.44 MHz) Example[1]						
$I_{VDDCORE}$	25°C	V		400		mA
I_{VDDIO}	25°C	V		25		mA
TDS-CDMA (76.8 MHz) Example[1, 2]						
$I_{VDDCORE}$	25°C	V		250		mA
I_{VDDIO}	25°C	V		15		mA
GSM (65 MHz) Example[1, 2]						
$I_{VDDCORE}$	25°C	V		175		mA
I_{VDDIO}	25°C	V		10		mA
TOTAL POWER DISSIPATION						
WCDMA (61.44 MHz)[1]	25°C	V		975		mW
CDMA2000 (61.44 MHz)[1]	25°C	V		800		mW
TD-SCDMA (76.8 MHz)[1, 2]	25°C	V		500		mW
GSM (65 MHz)[1, 2]	25°C	V		350		mW

[1] One input port, all six channels, and the relevant signal processing blocks are active.
[2] PLL is turned off for power savings.

GENERAL TIMING CHARACTERISTICS[1, 2]

Table 3.

Parameter		Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLKx Period (x = A, B, C, D)	Full	I	6.66			ns
t_{CLKL}	CLKx Width Low (x = A, B, C, D)	Full	IV	1.71	0.5 × t_{CLK}		ns
t_{CLKH}	CLKx Width High (x = A, B, C, D)	Full	IV	1.70	0.5 × t_{CLK}		ns
$t_{CLKSKEW}$	CLKA to CLKx Skew (x = B, C, D)	Full	IV	t_{CLK} − 1.3			ns
INPUT WIDEBAND DATA TIMING REQUIREMENTS		Full	IV				
t_{SI}	INx [15:0] to ↑CLKx Setup Time (x = A, B, C, D)	Full	IV	0.75			ns
t_{HI}	INx [15:0] to ↑CLKx Hold Time (x = A, B, C, D)	Full	IV	1.13			ns
t_{SEXP}	EXPx [2:0] to ↑CLKx Setup Time (x = A, B, C, D)	Full	IV	3.37			ns
t_{HEXP}	EXPx [2:0] to ↑CLKx Hold Time (x = A, B, C, D)	Full	IV	1.11			ns
t_{DEXP}	↑CLKx to EXPx[2:0] Delay (x = A, B, C, D)	Full	IV	5.98		10.74	ns
PARALLEL OUTPUT PORT TIMING REQUIREMENTS (MASTER)							
t_{DPREQ}	↑PCLK to ↑Px REQ Delay (x = A, B, C)	Full	IV	1.77		3.86	ns
t_{DPP}	↑PCLK to Px [15:0] Delay (x = A, B, C)	Full	IV	2.07		5.29	ns
t_{DPIQ}	↑PCLK to Px IQ Delay (x = A, B, C)	Full	IV	0.48		5.49	ns
t_{DPCH}	↑PCLK to Px CH[2:0] Delay (x = A, B, C)	Full	IV	0.38		5.35	ns
t_{DPGAIN}	↑PCLK to Px Gain Delay (x = A, B, C)	Full	IV	0.23		4.95	ns
t_{SPA}	Px ACK to ↑PCLK Setup Time (x = A, B, C)	Full	IV	4.59			ns
t_{HPA}	Px ACK to ↑PCLK Hold Time (x = A, B, C)	Full	IV	0.90			ns
PARALLEL OUTPUT PORT TIMING REQUIREMENTS (SLAVE)							
t_{PCLK}	PCLK Period	Full	IV	5.0			ns
t_{PCLKL}	PCLK Low Period	Full	IV	1.7	0.5 × t_{PCLK}		ns
t_{PCLKH}	PCLK High Period	Full	IV	0.7	0.5 × t_{PCLK}		ns
t_{DPREQ}	↑PCLK to ↑Px REQ Delay (x = A, B, C)	Full	IV	4.72		8.87	ns
t_{DPP}	↑PCLK to Px [15:0] Delay (x = A, B, C)	Full	IV	4.8		8.48	ns
t_{DPIQ}	↑PCLK to Px IQ Delay (x = A, B, C)	Full	IV	4.83		10.94	ns
t_{DPCH}	↑PCLK to Px CH[2:0] Delay (x = A, B, C)	Full	IV	4.88		10.09	ns
t_{DPGAIN}	↑PCLK to Px Gain Delay (x = A, B, C)	Full	IV	5.08		11.49	ns
t_{SPA}	Px ACK to ↓PCLK Setup Time (x = A, B, C)	Full	IV	6.09			ns
t_{HPA}	Px ACK to ↓PCLK Hold Time (x = A, B, C)	Full	IV	1.0			ns
MISC PINS TIMING REQUIREMENTS							
t_{RESET}	$\overline{\text{RESET}}$ Width Low	Full	IV	30			ns
t_{DIRP}	CPUCLK/SCLK to $\overline{\text{IRP}}$ Delay	Full	V		7.5		ns
t_{SSYNC}	SYNC(0, 1, 2, 3) to ↑CLKA Setup Time	Full	IV	0.87			ns
t_{HSYNC}	SYNC(0, 1, 2, 3) to ↑CLKA Hold Time	Full	IV	0.67			ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V and the VDDIO range of 3.0 V to 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.

MICROPORT TIMING CHARACTERISTICS[1, 2]

Table 4.

Parameter		Temp	Test Level	Min	Typ	Max	Unit
MICROPORT CLOCK TIMING REQUIREMENTS							
t_{CPUCLK}	CPUCLK Period	Full	IV	10.0			ns
$t_{CPUCLKL}$	CPUCLK Low Time	Full	IV	1.53	0.5 × t_{CPUCLK}		ns
$t_{CPUCLKH}$	CPUCLK High Time	Full	IV	1.70	0.5 × t_{CPUCLK}		ns
INM MODE WRITE TIMING (MODE = 0)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	0.80			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.09			ns
t_{SAM}	Address/Data to ↑CPUCLK Setup Time	Full	IV	0.76			ns
t_{HAM}	Address/Data to ↑CPUCLK Hold Time	Full	IV	0.20			ns
t_{DRDY}	↑CPUCLK to RDY ($\overline{DTACK}$) Delay	Full	IV	3.51		6.72	ns
t_{ACC}	Write Access Time	Full	IV	3 × t_{CPUCLK}		9 × t_{CPUCLK}	ns
INM MODE READ TIMING (MODE = 0)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	1.00			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.03			ns
t_{SAM}	Address to ↑CPUCLK Setup Time	Full	IV	0.80			ns
t_{HAM}	Address to ↑CPUCLK Hold Time	Full	IV	0.20			ns
t_{DD}	↑CPUCLK to Data Delay	Full	V		5.0		ns
t_{DRDY}	↑CPUCLK to RDY ($\overline{DTACK}$) Delay	Full	IV	4.50		6.72	ns
t_{ACC}	Read Access Time	Full	IV	3 × t_{CPUCLK}		9 × t_{CPUCLK}	ns
MNM MODE WRITE TIMING (MODE = 1)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	1.00			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.00			ns
t_{SAM}	Address/Data to ↑CPUCLK Setup Time	Full	IV	0.00			ns
t_{HAM}	Address/Data to ↑CPUCLK Hold Time	Full	IV	0.57			ns
t_{DDTACK}	↑CPUCLK to $\overline{DTACK}$ (RDY) Delay	Full	IV	4.10		5.72	ns
t_{ACC}	Write Access Time	Full	IV	3 × t_{CPUCLK}		9 × t_{CPUCLK}	ns
MNM MODE READ TIMING (MODE = 1)							
t_{SC}	Control[3] to ↑CPUCLK Setup Time	Full	IV	1.00			ns
t_{HC}	Control[3] to ↑CPUCLK Hold Time	Full	IV	0.00			ns
t_{SAM}	Address to ↑CPUCLK Setup Time	Full	IV	0.00			ns
t_{HAM}	Address to ↑CPUCLK Hold Time	Full	IV	0.57			ns
t_{DD}	CPUCLK to Data Delay	Full	V		5.0		ns
t_{DDTACK}	↑CPUCLK to $\overline{DTACK}$ (RDY) Delay	Full	IV	4.20		6.03	ns
t_{ACC}	Read Access Time	Full	IV	3 × t_{CPUCLK}		9 × t_{CPUCLK}	ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V and the VDDIO range of 3.0 V to 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.
[3] Specification pertains to control signals: R/$\overline{W}$ ($\overline{WR}$), $\overline{DS}$ ($\overline{RD}$), and $\overline{CS}$.

SERIAL PORT TIMING CHARACTERISTICS[1, 2, 3]

Table 5.

Parameter		Temp	Test Level	Min	Typ	Max	Unit
SERIAL PORT CLOCK TIMING REQUIREMENTS							
t_{SCLK}	SCLK Period	Full	IV	10.0			ns
t_{SCLKL}	SCLK Low Time	Full	IV	1.60	0.5 × t_{SCLK}		ns
t_{SCLKH}	SCLK High Time	Full	IV	1.60	0.5 × t_{SCLK}		ns
SPI PORT CONTROL TIMING REQUIREMENTS (MODE = 0)							
t_{SSDI}	SDI to ↑SCLK Setup Time	Full	IV	1.30			ns
t_{HSDI}	SDI to ↑SCLK Hold Time	Full	IV	0.40			ns
t_{SSCS}	$\overline{SCS}$ to ↑SCLK Setup Time	Full	IV	4.12			ns
t_{HSCS}	$\overline{SCS}$ to ↑SCLK Hold Time	Full	IV	−2.78			ns
t_{DSDO}	↑SCLK to SDO Delay Time	Full	IV	4.28		7.96	ns
SPORT MODE CONTROL TIMING REQUIREMENTS (MODE = 1)							
t_{SSDI}	SDI to ↑SCLK Setup Time	Full	IV	0.80			ns
t_{HSDI}	SDI to ↑SCLK Hold Time	Full	IV	0.40			ns
t_{SSRFS}	SRFS to ↓SCLK Setup Time	Full	IV	1.60			ns
t_{HSRFS}	SRFS to ↓SCLK Hold Time	Full	IV	−0.13			ns
t_{SSTFS}	STFS to ↓SCLK Setup Time	Full	IV	1.60			ns
t_{HSTFS}	STFS to ↑SCLK Hold Time	Full	IV	−0.30			ns
t_{SSCS}	$\overline{SCS}$ to ↑SCLK Setup Time	Full	IV	4.12			ns
t_{HSCS}	$\overline{SCS}$ to ↑SCLK Hold Time	Full	IV	−2.76			ns
t_{DSDO}	↑SCLK to SDO Delay Time	Full	IV	4.29		7.95	ns

[1] All timing specifications are valid over the VDDCORE range of 1.7 V to 1.9 V and the VDDIO range of 3.0 V to 3.6 V.
[2] C_{LOAD} = 40 pF on all outputs, unless otherwise noted.
[3] SCLK rise/fall time should be 3 ns maximum.

EXPLANATION OF TEST LEVELS FOR SPECIFICATIONS

Table 6.

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C, and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter guaranteed by design and analysis.
V	Parameter is typical value only.
VI	100% production tested at 25°C, and sampled tested at temperature extremes.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
ELECTRICAL	
VDDCORE Supply Voltage (Core Supply)	2.2 V
VDDIO Supply Voltage (Ring or IO Supply)	4.0 V
Input Voltage	−0.3 to +3.6 V (Not 5 V Tolerant)
Output Voltage	−0.3 to VDDIO + 0.3 V
Load Capacitance	200 pF
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

256-ball CSP_BGA package:

θ_{JA} = 25.4°C /W, no airflow

θ_{JA} = 23.3°C /W, 0.5 m/s airflow

θ_{JA} = 22.6°C /W, 1.0 m/s airflow

θ_{JA} = 21.9°C /W, 2.0 m/s airflow

Thermal measurements made in the horizontal position on a 4-layer board with vias.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	GND	INC3	IND4	IND7	CLKD	CLKC	IND11	GND	VDDCORE	IND14	IND15	SYNC1	TDO	PBGAIN	PB11	GND	A
B	IND0	VDDIO	INC2	IND5	IND6	IND8	IND10	IND12	IND13	INC14	SYNC3	SYNC0	$\overline{\text{TRST}}$	PBCH2	VDDIO	PB12	B
C	EXPA1	EXPD1	INC0	INC1	IND3	INC5	IND9	INC10	INC13	SYNC2	TMS	TCLK	PBCH0	PB8	PB15	PB10	C
D	EXPB0	EXPC2	EXPC1	EXPD0	IND2	INC4	INC7	INC9	INC12	TDI	PBCH1	PBIQ	PB14	PB9	PB13	PACH1	D
E	INA14	INA15	EXPA0	LVDS_RSET	GND	IND1	INC6	INC8	INC11	INC15	PBREQ	PBACK	PB4	PB5	PB1	PCLK	E
F	INA12	INA13	EXPB1	EXPC0	EXPD2	GND	VDDIO	VDDIO	VDDIO	VDDIO	GND	PB6	PB0	PB7	PAREQ	PA0	F
G	INA11	INB13	INB15	EXPB2	EXPA2	VDDCORE	GND	GND	GND	GND	VDDCORE	PB3	PAGAIN	PB2	PACH0	PA2	G
H	VDDCORE	INA10	INB12	INB11	INB14	VDDCORE	GND	GND	GND	GND	VDDCORE	PACH2	PAIQ	PAACK	PA1	GND	H
J	GND	INA9	INB10	INB8	INB9	VDDCORE	GND	GND	GND	GND	VDDCORE	PA3	PA7	PA5	PA4	VDDCORE	J
K	CLKA	INA8	INA7	INB6	INB7	VDDCORE	GND	GND	GND	GND	VDDCORE	PA12	PA15	PA9	PA8	PA6	K
L	CLKB	INA6	INB4	INB1	INB3	GND	VDDIO	VDDIO	VDDIO	VDDIO	GND	PC3	PCACK	PCCH1	PA13	PA10	L
M	INA5	INB5	INB2	INB0	GND	$\overline{\text{DTACK}}$ (RDY, SDO)	D13	D15	D5	A5	PC12	PC7	PC2	PC0	PCCH0	PA11	M
N	INA4	INA3	INA0	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$, STFS)	$\overline{\text{CS}}$ ($\overline{\text{SCS}}$)	CHIPID2	D12	D2	D1	A4	A0 (SDI)	PC15	PC5	PC1	PCCH2	PA14	N
P	INA2	INA1	$\overline{\text{RESET}}$	$\overline{\text{DS}}$ ($\overline{\text{RD}}$, SRFS)	SMODE	CHIPID3	GND	D9	D4	A6	A2	PC11	PC10	PC4	PCIQ	PCGAIN	P
R	CPUCLK (SCLK)	VDDIO	MSB_FIRST	EXT_FILTER	CHIPID1	D14	D10	D11	D6	D0	A3	A1	PC9	PC6	VDDIO	PCREQ	R
T	GND	$\overline{\text{IRP}}$	MODE	CHIPID0	D7	D8	D3	VDDCORE	GND	GND	A7	PC14	PC13	PC8	GND	GND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

■ = VDDCORE ■ = VDDIO ■ = GROUND

04998-0-002

Figure 2. CSP_BGA Pin Configuration

Table 8. Pin Function Descriptions

Mnemonic	Type	Pin No.	Function
POWER SUPPLY			
VDDCORE	Power	See Table 9	1.8 V Digital Core Supply.
VDDIO	Power	See Table 9	3.3 V Digital I/O Supply.
GND	Ground	See Table 9	Digital Core and I/O Ground.
INPUT (ADC) PORTS (CMOS/LVDS)			
CLKA	Input	K1	Clock for Input Port A. Used to clock INA[15:0] and EXPA[2:0] data. Additionally, this clock is used to drive internal circuitry and PLL clock multiplier.
CLKB	Input	L1	Clock for Input Port B. Used to clock INB[15:0] and EXPB[2:0] data.
CLKC	Input	A6	Clock for Input Port C. Used to clock INC[15:0] and EXPC[2:0] data.
CLKD	Input	A5	Clock for Input Port D. Used to clock IND[15:0] and EXPD[2:0] data.
INA[0:15]	Input	See Table 9	Input Port A (Parallel).
INB[0:15]	Input	See Table 9	Input Port B (Parallel).
INC[0:15]	Input	See Table 9	Input Port C (Parallel).
IND[0:15]	Input	See Table 9	Input Port D (Parallel).
EXPA[0:2]	Bidirectional	E3, C1, G5	Exponent Bus Input Port A. Gain control output.

Mnemonic	Type	Pin No.	Function
EXPB[0:2]	Bidirectional	D1, F3, G4	Exponent Bus Input Port B. Gain control output.
EXPC[0:2]	Bidirectional	F4, D3, D2	Exponent Bus Input Port C. Gain control output.
EXPD[0:2]	Bidirectional	D4, C2, F5	Exponent Bus Input Port D. Gain control output.
CLKA, CLKB	Input	K1, L1	LVDS Differential Clock for LVDS_A Input Port (LVDS_CLKA+, LVDS_CLKA−).
CLKC, CLKD	Input	A6, A5	LVDS Differential Clock for LVDS_C Input Port (LVDS_CLKC+, LVDS_CLKC−).
INA[0:15], INB[0:15]	LVDS Input	See Table 9	In LVDS input mode, INA[0:15] and INB[0:15] form a differential pair LVDS_A+[0:15] (positive node) and LVDS_A−[0:15] (negative node), respectively.
INC[0:15], IND[0:15]	LVDS Input	See Table 9	In LVDS input mode, INC[0:15] and IND[0:15] form a differential pair LVDS_C+[0:15] (positive node) and LVDS_C−[0:15] (negative node), respectively.
OUTPUT PORTS			
PCLK	Bidirectional	E16	Parallel Output Port Clock. Master mode output, and slave mode input.
PA[0:15]	Output	See Table 9	Parallel Output Port A Data Bus.
PACH[0:2]	Output	G15, D16, H12	Channel Indicator Output Port A.
PAIQ	Output	H13	Parallel Port A I/Q Data Indicator. Logic 1 indicates I data on data bus.
PAGAIN	Output	G13	Parallel Port A Gain Word Output Indicator. Logic 1 indicates gain word on data bus.
PAACK	Input	H14	Parallel Port A Acknowledge (Active High).
PAREQ	Output	F15	Parallel Port A Request (Active High).
PB[0:15]	Output	See Table 9	Parallel Output Port B Data Bus.
PBCH[0:2]	Output	C13, D11, B14	Channel Indicator Output Port B.
PBIQ	Output	D12	Parallel Port B I/Q Data Indicator. Logic 1 indicates I data on data bus.
PBGAIN	Output	A14	Parallel Port B Gain Word Output Indicator. Logic 1 indicates gain word on data bus.
PBACK	Input	E12	Parallel Port B Acknowledge (Active High).
PBREQ	Output	E11	Parallel Port B Request (Active High).
PC[0:15]	Output	See Table 9	Parallel Output Port C Data Bus.
PCCH[0:2]	Output	M15, L14, N15	Channel Indicator Output Port C.
PCIQ	Output	P15	Parallel Port C I/Q Data Indicator. Logic 1 indicates I data on data bus.
PCGAIN	Output	P16	Parallel Port C Gain Word Output Indicator. Logic 1 indicates gain word on data bus.
PCACK	Input	L13	Parallel Port C Acknowledge (Active High).
PCREQ	Output	R16	Parallel Port C Request (Active High).

MISC PINS			
$\overline{\text{RESET}}$	Input	P3	Master Reset (Active Low).
$\overline{\text{IRP}}$[1]	Output	T2	Interrupt Pin (Open Drain Output, Needs External Pull-Up Resistor 1 kΩ).
SYNC[0:3]	Input	B12, A12, C10, B11	Synchronization Inputs. SYNC pins are independent of channels or input ports and independent of each other.
LVDS_RSET	Input	E4	LVDS Resistor Set Pin (Analog Pin). See Design Notes.
EXT_FILTER	Input	R4	PLL Loop Filter (Analog Pin). See Design Notes.
MICROPORT CONTROL			
D[0:15]	Bidirectional	See Table 9	Bidirectional Microport Data. This bus is three-stated when $\overline{\text{CS}}$ is high.
A[0:7]	Input	See Table 9	Microport Address Bus.
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	Input	P4	Active Low Data Strobe when MODE = 1. Active low read strobe when MODE = 0.
$\overline{\text{DTACK}}$ (RDY)[1]	Output	M6	Active Low Data Acknowledge when MODE = 1. Microport status pin when MODE = 0. Open drain output, needs external pull-up resistor 1 kΩ.
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	Input	N4	Read/Write Strobe when MODE = 1. Active low write strobe when MODE = 0.
MODE	Input	T3	Mode Select Pin. When SMODE = 0: Logic 0 = Intel mode; Logic 1 = Motorola mode. When SMODE = 1: Logic 0 = SPI mode; Logic 1 = SPORT mode.
$\overline{\text{CS}}$	Input	N5	Active Low Chip Select. Logic 1 three-states the microport data bus.
CPUCLK	Input	R1	Microport CLK Input (Input Only).
CHIPID[0:3]	Input	T4, R5, N6, P6	Chip ID Input Pins.

Mnemonic	Type	Pin No.	Function
SERIAL PORT CONTROL			
SCLK	Input	R1	Serial Clock.
SDO[1]	Output	M6	Serial Port Data Output (Open drain output, needs external pull-up resistor 1KΩ).
SDI[2]	Input	N11	Serial Port Data Input.
STFS	Input	N4	Serial Transmit Frame Sync.
SRFS	Input	P4	Serial Receive Frame Sync.
$\overline{\text{SCS}}$	Input	N5	Serial Chip Select.
MSB_FIRST	Input	R3	Select MSB First into SDI Pin and MSB First Out of SDO Pin. Logic 0 = MSB first; Logic 1 = LSB first.
SMODE	Input	P5	Serial Mode Select. Pull high when serial port is used and low when microport is used.
JTAG			
$\overline{\text{TRST}}$[1]	Input	B13	Test Reset Pin. Pull low when JTAG is not used.
TCLK[2]	Input	C12	Test Clock.
TMS[1]	Input	C11	Test Mode Select.
TDO	Output	A13	Test Data Output. Three-stated when JTAG is in reset.
TDI[1]	Input	D10	Test Data Input.

[1] Pin with a pull-up resistor of nominal 70 kΩ.
[2] Pin with a pull-down resistor of nominal 70 kΩ.

PIN LISTING FOR POWER, GROUND, DATA, AND ADDRESS BUSES

Table 9.

Mnemonic	Pin No.
VDDCORE	A9, G6, G11, H1, H6, H11, J6, J11, J16, K6, K11, T8
VDDIO	B2, B15, F7, F8, F9, F10, L7, L8, L9, L10, R2, R15
GND	A1, A8, A16, E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, H16, J1, J7, J8, J9, J10, K7, K8, K9, K10, L6, L11, M5, P7, T1, T9, T10, T15, T16
INA[0:15]	N3, P2, P1, N2, N1, M1, L2, K3, K2, J2, H2, G1, F1, F2, E1, E2
INB[0:15]	M4, L4, M3, L5, L3, M2, K4, K5, J4, J5, J3, H4, H3, G2, H5, G3
INC[0:15]	C3, C4, B3, A2, D6, C6, E7, D7, E8, D8, C8, E9, D9, C9, B10, E10
IND[0:15]	B1, E6, D5, C5, A3, B4, B5, A4, B6, C7, B7, A7, B8, B9, A10, A11
PA[0:15]	F16, H15, G16, J12, J15, J14, K16, J13, K15, K14, L16, M16, K12, L15, N16, K13
PB[0:15]	F13, E15, G14, G12, E13, E14, F12, F14, C14, D14, C16, A15, B16, D15, D13, C15
PC[0:15]	M14, N14, M13, L12, P14, N13, R14, M12, T14, R13, P13, P12, M11, T13, T12, N12
D[0:15]	R10, N9, N8, T7, P9, M9, R9, T5, T6, P8, R7, R8, N7, M7, R6, M8
A[0:7]	N11, R12, P11, R11, N10, M10, P10, T11

TIMING DIAGRAMS

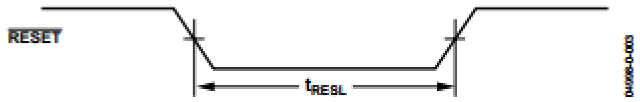


Figure 3. Reset Timing Requirements

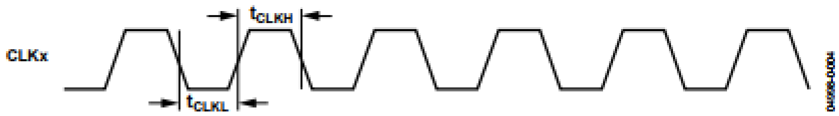


Figure 4. CLK Switching Characteristics
(x = A, B, C, D for Individual Input Ports)

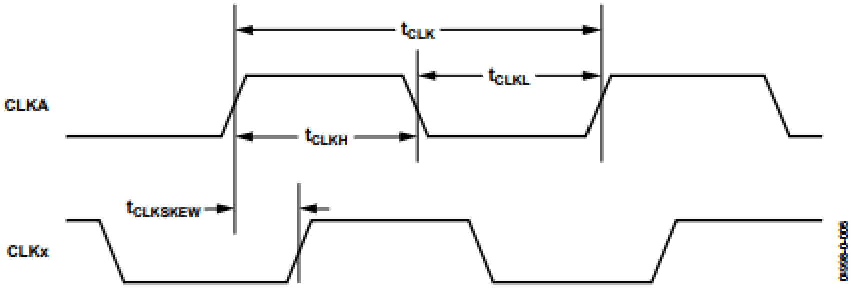


Figure 5. CLK Skew Characteristics
(x = B, C, D for Individual Input Ports)

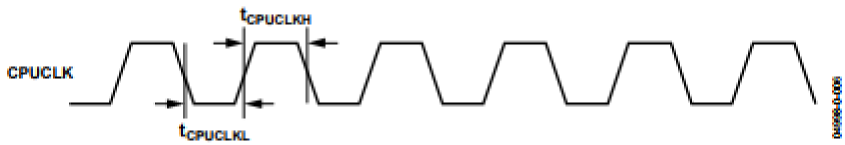


Figure 6. CPUCLK Switching Characteristics

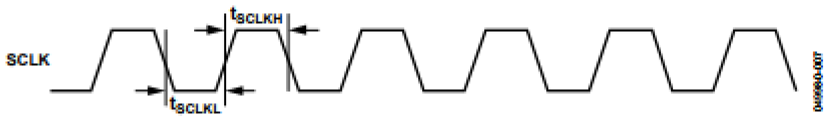


Figure 7. SCLK Switching Characteristics

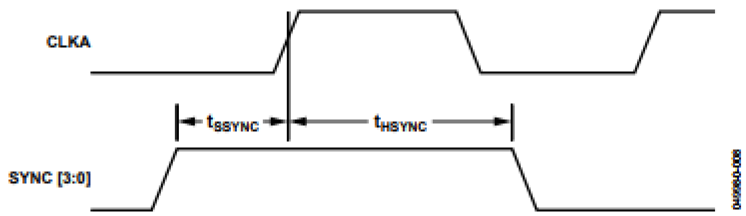


Figure 8. SYNC Timing Inputs

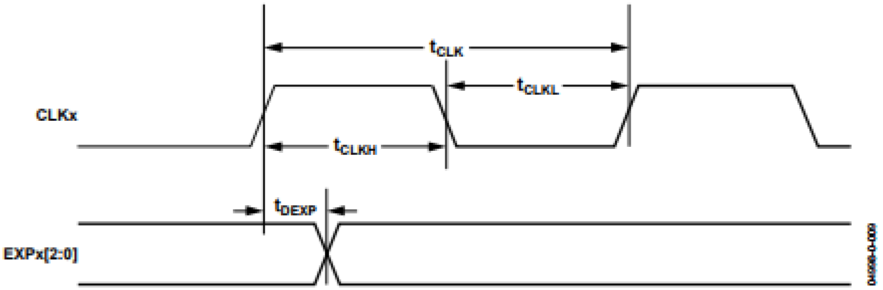


Figure 9. Gain Control Word Output Switching Characteristics (x = A, B, C, D for Individual Input Ports)

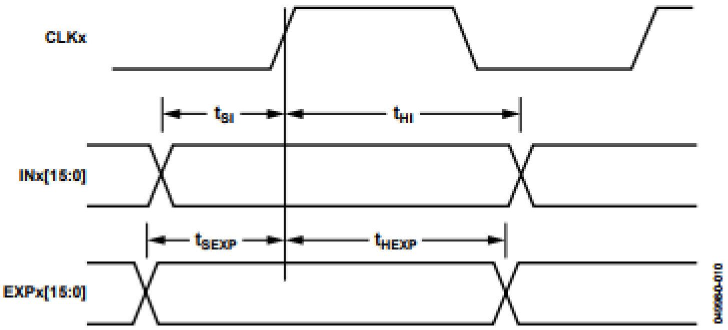


Figure 10. Input Port Timing for Data (x = A, B, C, D for Individual Input Ports)

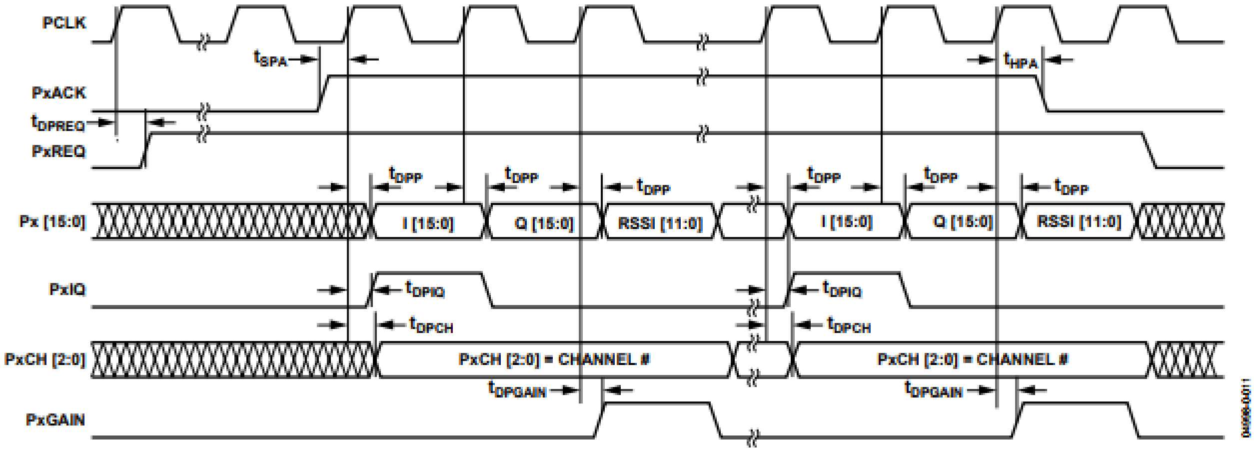


Figure 11. Master Mode PxACK to PCLK Switching Characteristics (x = A, B, C, D for Individual Output Ports)

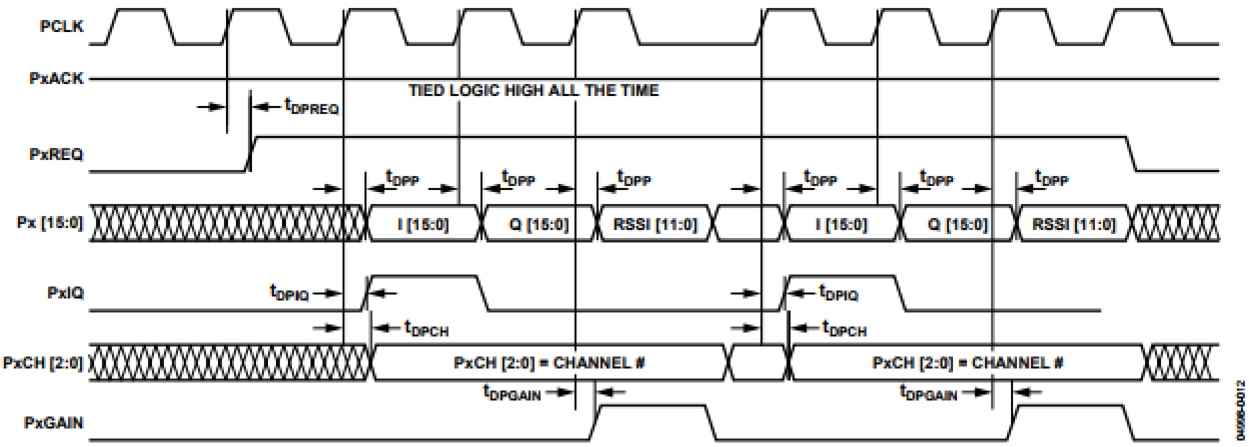
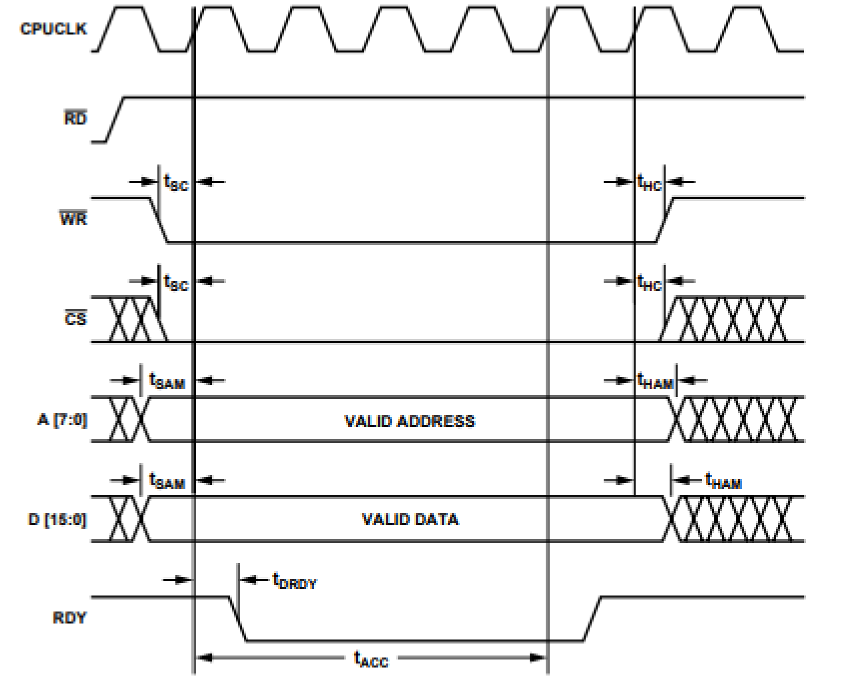
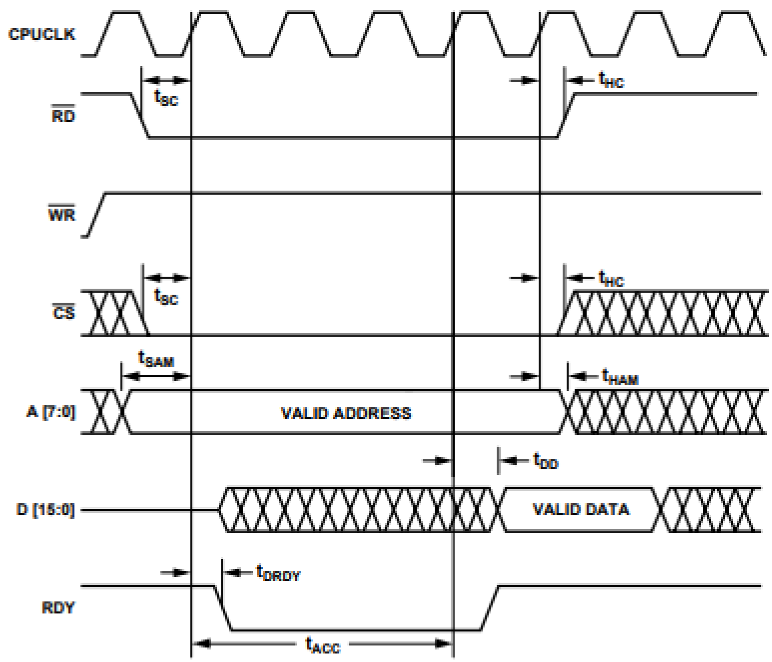


Figure 12. Master Mode PxREQ to PCLK Switching Characteristics



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

Figure 13. INM Microport Write Timing Requirements



NOTE:
t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. IT CAN VARY FROM 3 TO 9 CPUCLK CYCLES.

Figure 14. INM Microport Read Timing Requirements

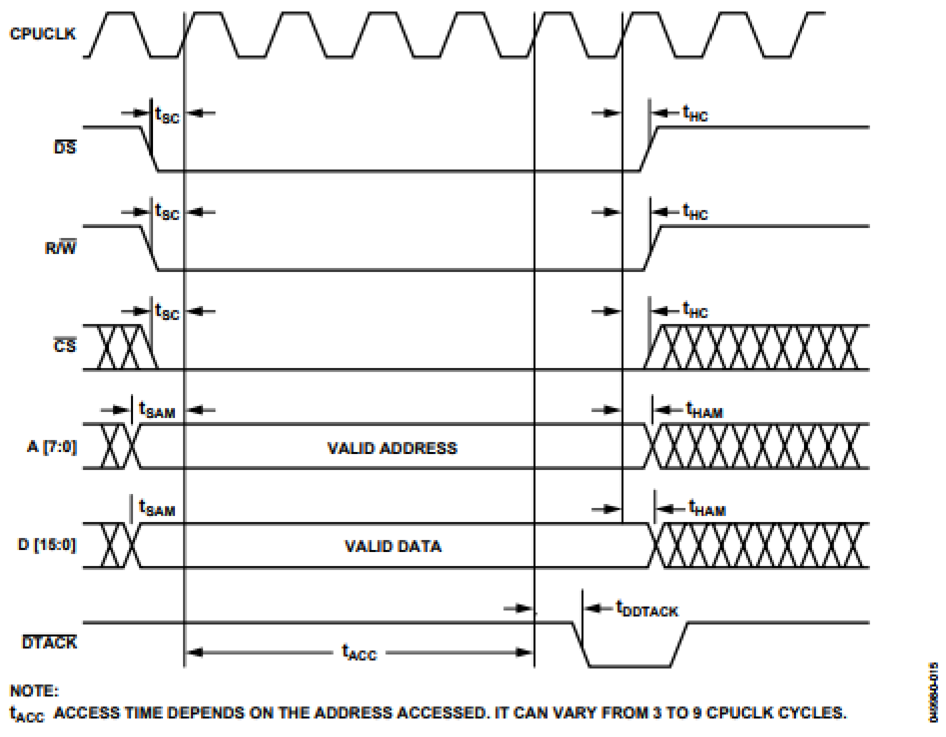


Figure 15. MNM Microport Write Timing Requirements

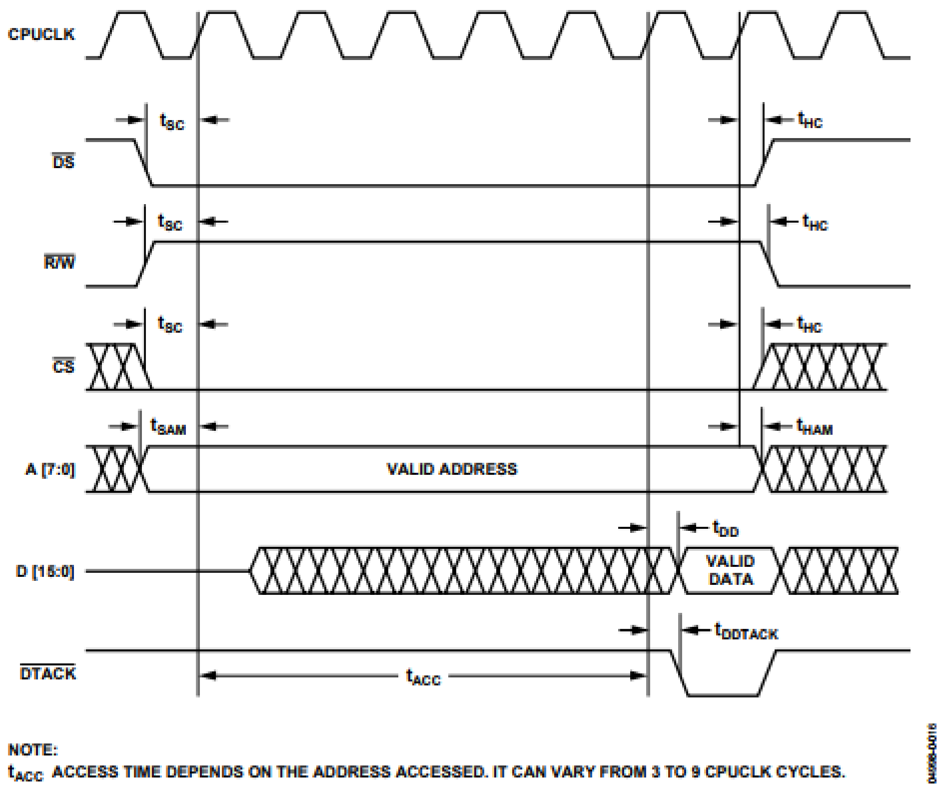


Figure 16. MNM Microport Read Timing Requirements

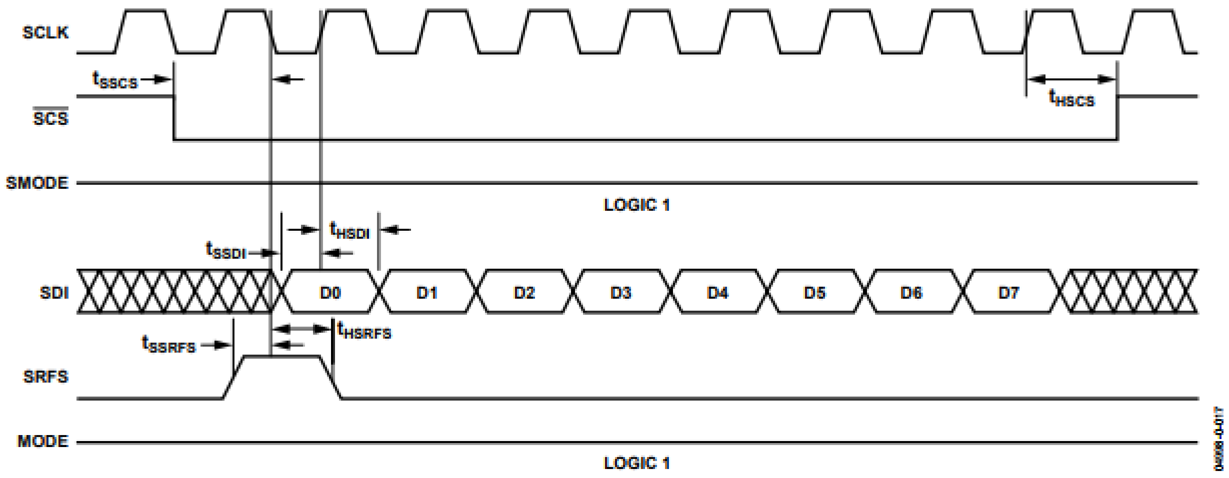


Figure 17. SPORT Mode Write Timing Characteristics

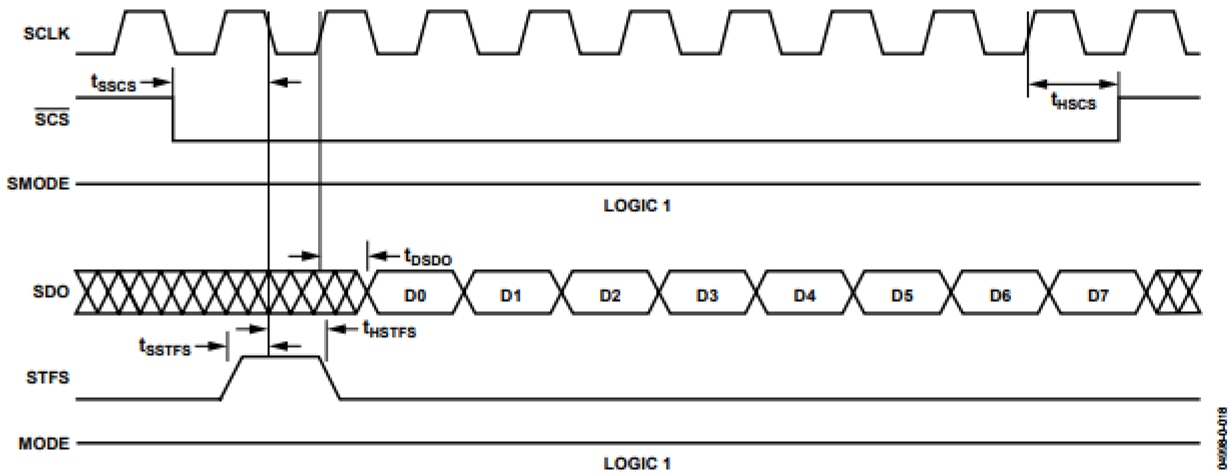


Figure 18. SPORT Mode Read Timing Characteristics

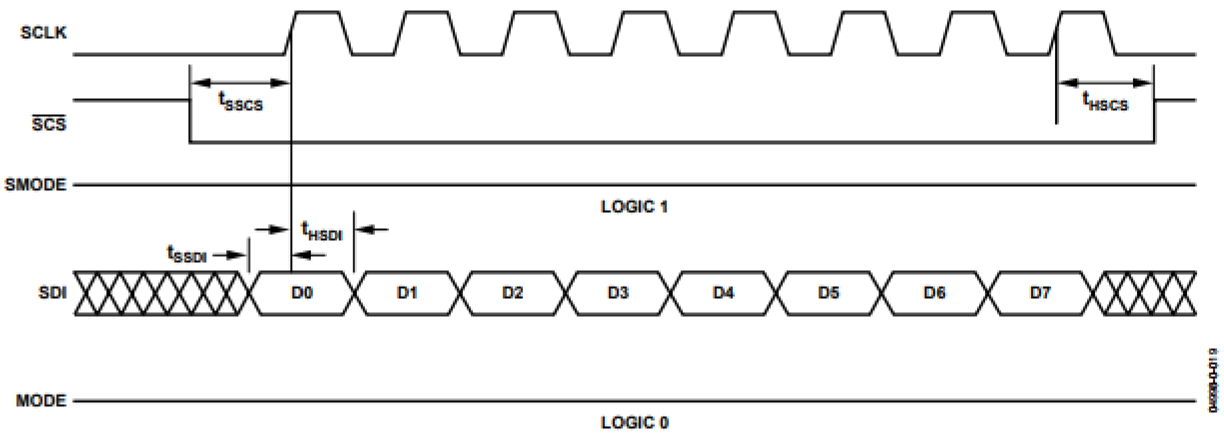


Figure 19. SPI Mode Write Timing Characteristics

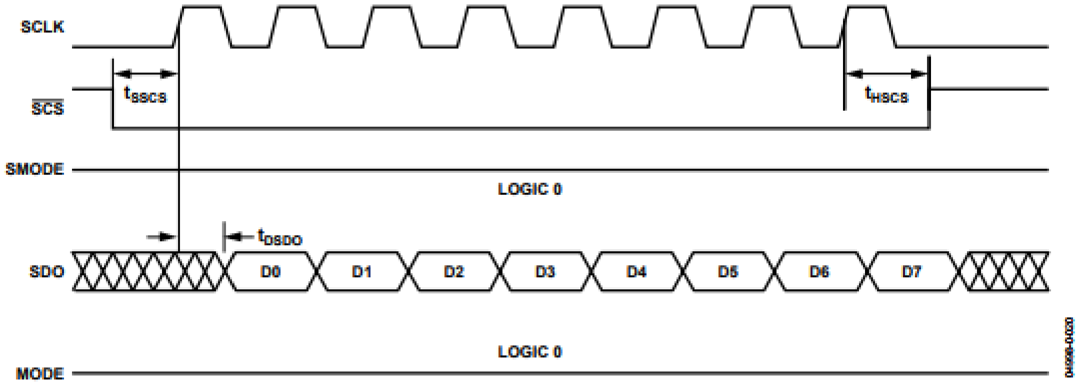


Figure 20. SPI Mode Read Timing Characteristics

THEORY OF OPERATION

ADC INPUT PORT

The AD6636 features four identical, independent high speed ADC input ports named A, B, C, and D. These input ports have the flexibility to allow independent inputs, diversity inputs, or complex I/Q inputs. Any of the ADC input ports can be routed to any of the six tuner channels; that is, any of the six. The AD6636 channels can receive input data from any of the input ports. Time-multiplexed inputs on a single port are not supported in the AD6636.

These four input ports can operate at up to 150 MSPS. Each input port has its own clock (CLKA, CLKB, CLKC, and CLKD) used for registering input data into the AD6636. To allow slow input rates while providing fast processing clock rates, the AD6636 contains an internal PLL clock multiplier that supplies the internal signal processing clock. CLKA is used as an input to the PLL clock multiplier. Additional programmability allows the input data to be clocked into the part either on the rising edge or the falling edge of the input clock.

In addition, the front end of the AD6636 contains circuitry that enables high speed signal-level detection, gain control, and quadrature I/Q correction. This is accomplished with a unique high speed level-detection circuit that offers minimal latency and maximum flexibility to control all four input signals (typically ADC inputs) individually. The input ports also provide input power-monitoring functions via various modes and magnitude and phase I/Q correction blocks. See the Quadrature I/Q Correction Block section for details.

The 3-exponent bits are shared with the gain range control bits in the hardware. When floating-point ADCs are not used, these three pins on each ADC input port can be used as gain range control output bits.

Input Timing

The data from each high speed input port is latched either on the rising edge or the falling edge of the port's individual CLKx (where x stands for A, B, C, or D input ports). The ADC clock invert bit in ADC clock control register selects the edge of the clock (rising or falling) used to register input data into the AD6636.

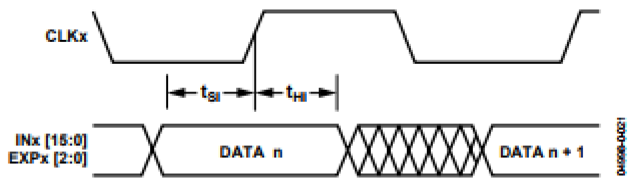


Figure 21. Input Data Timing Requirements (Rising Edge of Clock, x = A, B, C, or D for Four Input Ports)

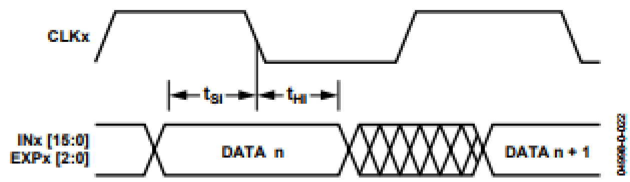


Figure 22. Input Data Timing Requirements (Falling Edge of Clock, x = A, B, C, or D for Four Input Ports)

Each individual processing channel can receive input data from any of the four input ports individually. This is controlled using 3-bit crossbar mux-select bit words in the ADC input control register. Each individual channel has a similar 3-bit selection. In addition to the four input ports, an internal test signal (PN—pseudorandom noise sequence) can also be selected. This internal test signal is discussed in the User-Configurable, Built-In Self-Test (BIST) section.

Input Data Format

Each input port consists of a 16-bit mantissa and a 3-bit exponent (16 + 3 floating-point input, or up to 16-bit fixed-point input). When interfacing to standard fixed-point ADCs, the exponent bit should either be connected to ground or be programmed as outputs for gain control output. If connected to a floating-point ADC (also called gain ranging ADC), the exponent bits from the ADC can be connected to the input exponent bits of the AD6636. The mantissa data format is twos complement, and the exponent is unsigned binary.

The clock signals (CLKA, CLKB, CLKC, and CLKD) can operate at up to 150 MHz. In applications using high speed ADCs, the ADC sample clock, data valid, or data-ready strobe are typically used to clock the AD6636.

Connection to Fixed-Point ADC

For fixed-point ADCs, the AD6636 exponent inputs, EXP[2:0], are not typically used and should be tied low. Alternatively, because these pins are shared with gain range control bits, if the gain ranging block is used, these pins can be used as outputs of the gain range control block. The ADC outputs are tied directly to the AD6636 inputs, MSB justified. Therefore, for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6636. Figure 23 shows a typical interconnection.

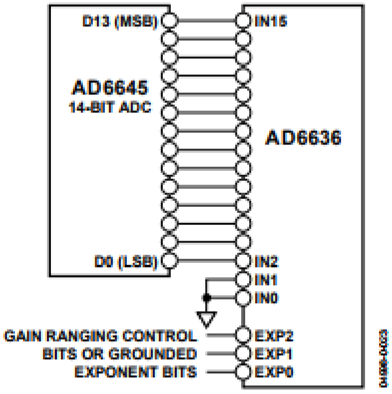


Figure 23. Typical Interconnection of the AD6645 Fixed-Point ADC and AD6636

Scaling with Floating-Point ADC

An example of the exponent control feature combines the AD6600 and the AD6636. The AD6600 is an 11-bit ADC with three bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the three bits of the relative signal strength indicator (RSSI) are the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for details.

Table 10. Weighting Factors for Different Exp[2:0] Values

ADC Input Level	AD6636 Exp[2:0]	Data Divide-By	Signal Attenuation (dB)
Largest	000 (0)	/1 (>> 0)	0
	001 (1)	/2 (>> 1)	6
	010 (2)	/4 (>> 2)	12
	011 (3)	/8 (>> 3)	18
	100 (4)	/16 (>> 4)	24
	101 (5)	/32 (>> 5)	30
	110 (6)	/64 (>> 6)	36
Smallest	111 (7)	/128 (>> 7)	42

Complex (I/Q) Input Ports

The four individual ADC input ports of the AD6636 can be configured to function as two complex input ports. Additionally, if required, only two input ports can be made to function as a complex port, while the remaining two input ports function as real individual input ports.

In complex mode, Input Port A is paired with Input Port B to receive I and Q data, respectively. Similarly, Input Port C can be paired with Input Port D to receive I and Q data, respectively. These two pairings are controlled individually using Bit 24 and Bit 25 of the ADC input control register.

As explained previously, each individual channel can receive input signals from any of the four input ports using the crossbar mux select bits in the ADC input control register. In addition to the three bits, a 1-bit selection is provided for choosing the complex input port option for any individual channel. For example, if Channel 0 needs to receive complex input from Input Port A and Input Port B, the mux select bits should indicate Input Port A, and the complex input bit should be selected.

When the input ports are paired for complex input operation, only one set of exponent bits is driven externally with gain control output. Therefore, when Input Port A and Input Port B form a complex input, EXPA[2:0] are output and, similarly, for Input Port C and Input Port D, EXPC[2:0] are output.

LVDS Input Ports

The AD6636 input ports can be configured in CMOS mode or LVDS mode. In CMOS input mode, the four input ports can be configured as two complex input ports. In LVDS mode, two CMOS input ports are each combined to form one LVDS input port.

CMOS Input Port INA[15:0] and CMOS Input Port INB[15:0] form the positive and negative differential nodes, LVDS_A+[15:0] and LVDS_A−[15:0], respectively. Similarly, INC[15:0] and IND[15:0] form the positive and negative differential nodes, LVDS_C+[15:0] and LVDS_C− [15:0], respectively. CLKA and CLKB form the differential pair, Pin LVDS_CLKA+ and Pin LVDS_CLKA−. Similarly, CLKC and CLKD form the differential pair Pin LVDS_CLKC+ and Pin LVDS_CLKC−.

By default, the AD6636 powers up in CMOS mode and can be programmed to CMOS mode by using the CMOS mode bit (Bit 10 of the LVDS control register). Writing Logic 1 to Bit 8 of the LVDS control register enables an autocalibrate routine that calibrates the impedance of the LVDS pads to match the output impedance of the LVDS signal source impedance. The LVDS pads in the AD6636 have an internal impedance of 100 Ω across the differential signals; therefore, an external resistor is not required.

PLL CLOCK MULTIPLIER

In the AD6636, the input clock rate must be the same as the input data rate. In a typical digital downconverter architecture, the clock rate is a limitation on the number of filter taps that can be calculated in the programmable RAM coefficient filters (MRCF, DRCF, and CRCF). For slower ADC clock rates (or for any clock rate), this limitation can be overcome by using a PLL clock multiplier to provide a higher clock rate to the RCF filters. Using this clock multiplier, the internal signal processing clock rate can be increased up to 200 MHz. The CLKA signal is used as an input to the PLL clock multiplier.

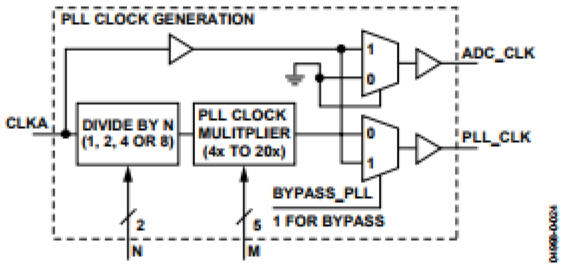


Figure 24. PLL Clock Generation

The PLL clock multiplier is programmable and uses input clock rates between 4 MHz and 150 MHz to give a system clock rate (output) of as high as 200 MHz.

The output clock rate is given by

$$PLL\_CLK = \frac{CLKA \times M}{N}$$

where:

CLKA is the Input Port A clock rate.

M is a 5-bit programmable multiplication factor.

N is a predivide factor.

M is a 5-bit number between 4 and 20 (both values included). *N* (predivide) can be 1, 2, 4, or 8. The multiplication factor *M* is programmed using a 5-bit PLL clock multiplier word in the ADC clock control register. A value outside the valid range of 4 to 20 bypasses the PLL clock multiplier and, therefore, the PLL clock is the same as the input clock. The predivide factor *N* is programmed using a 2-bit ADC pre-PLL clock divider word in the ADC clock control register, as listed in Table 11.

Table 11. PLL Clock Generation Predivider Control

Predivide Word [1:0]	Divide-by Value for the Clock
00	Divide-by-1, bypass
01	Divide-by-2
10	Divide-by-4
11	Divide-by-8

For the best signal processing advantage, the user should program the clock multiplier to give a system clock output as close as possible to, but not exceeding, 200 MHz. The internal blocks of the AD6636 that run off of the PLL clock are rated to run at a maximum of 200 MHz. The default power-up state for the PLL clock multiplier is the bypass state, where CLKA is passed on as the PLL clock.

ADC GAIN CONTROL

Each ADC input port has individual, high speed, gain-control logic circuitry. Such gain-control circuitry is useful in applications that involve large dynamic range inputs or in which gain ranging ADCs are employed. The AD6636 gain-control logic allows programmable upper and lower thresholds and a programmable dwell-time counter for temporal hysteresis.

Each input port has a 3-bit output from the gain control block. These three output pins are shared with the 3-bit exponent input pins for each input port. The operation is controlled by the gain control enable bit in the gain control register of the individual input ports. Logic 1 in this bit programs the EXP[2:0] pins as gain-control outputs, and Logic 0 configures the pins as input exponent pins. To avoid bus contention, these pins are set, by default, as input exponent pins.

Function

The gain-control block features a programmable upper threshold register and a lower threshold register. The ADC input data is compared to both these registers. If ADC input data is larger than the upper threshold register, then the gain control output is decremented by 1. If ADC input data is smaller than the lower threshold register, then the gain control output is incremented by 1. When decrementing the gain control output, the change is immediate. But when incrementing the output, a dwell-time register is used to delay the change. If the ADC input is larger than the upper threshold register value, the gain-control output is decremented to prevent overflow immediately.

When the ADC input is lower than the lower threshold register, a dwell timer is loaded with the value in the programmable, 20-bit, dwell-time register. The counter decrements once every input clock cycle, as long as the input signal remains below the lower threshold register value. If the counter reaches 1, the gain control output is incremented by 1. If the signal goes above the lower threshold register value, the gain adjustment is not made, and the normal comparison to lower and upper threshold registers is initiated once again. Therefore, the dwell timer provides temporal hysteresis and prevents the gain from switching continuously.

In a typical application, if the ADC signal goes below the lower threshold for a time greater than the dwell time, then the gain control output is incremented by 1. Gain control bits control the gain ranging block, which appears before the ADC in the signal chain. With each increment of the gain control output, gain in the gain-ranging block is increased by 6.02 dB. This increases the dynamic range of the input signal into the ADC by 6.02 dB. This gain is compensated for in the AD6636 by relinearizing (see the Relinearization section). Therefore, the AD6636 can increase the dynamic range of the ADC by 42 dB, provided that the gain-ranging block can support it.

Relinearization

The gain in the gain-ranging block (external) is compensated for by relinearizing, using the exponent bits, EXP[2:0], of the input port. For this purpose, the gain control bits are connected to the EXP[2:0] bits, providing an attenuation of 6.02 dB for every increase in the gain control output. After the gain in the external gain-ranging block and the attenuation in the AD6636 (using EXP bits), the signal gain is essentially unchanged. The only change is the increase in the dynamic range of the ADC.

External gain-ranging blocks or gain-ranging ADCs have a delay associated with changing the gain of the signal. Typically, these delays can be up to 14 clock cycles. The gain change in the AD6636 (via EXP[2:0]) must be synchronized with the gain change in the gain-ranging block (external). This is allowed in the AD6636 by providing a flexible delay, programmable 6-bit word in the gain control register. The value in this 6-bit word gives the delay in input clock cycles. A programmable pipeline delay given by the 6-bit value (maximum delay of 63 clock cycles) is placed between the gain control output and the EXP[2:0] input. Therefore, the external gain-ranging block's settling delays are compensated for in the AD6636.

Note that any gain changes that are initiated during the relinearization period are ignored. For example, if the AD6636 detects that a gain adjustment is required during the relinearization period of a previous gain adjustment, then the new adjustment is ignored.

Setting Up the Gain Control Block

To set up the gain control block for individual input ports, the individual upper threshold registers and lower threshold registers should be written with appropriate values. The 10-bit values written into upper and lower threshold registers are compared to the 10 MSB bits of the absolute magnitude calculated using the input port data. The 20-bit dwell timer register should have the appropriate number of clock cycles to provide temporal hysteresis.

A 6-bit relinearization pipeline delay word is set to synchronize with the settling delay in the external gain ranging circuitry. Finally, the gain control enable bit is written with Logic 1 to activate the gain control block. On enabling, the gain control output bits are made 000 (output on EXP[2:0] pins), which represent the minimum gain for the external gain-ranging circuitry and corresponding minimum attenuation during relinearization. The normal functioning takes over, as explained previously in this section.

Complex Inputs

For complex inputs (formed by pairing two input ports), only one set of EXP[2:0] pins should be used as the gain control output. For the pair of Input Port A and Input Port B, gain control circuitry for Input Port A is active, and EXPA[2:0] should be connected externally as the gain control output. The gain control circuitry for Input Port B is not activated (shut down), and EXPB[2:0] is forced to be equal to EXP[2:0].

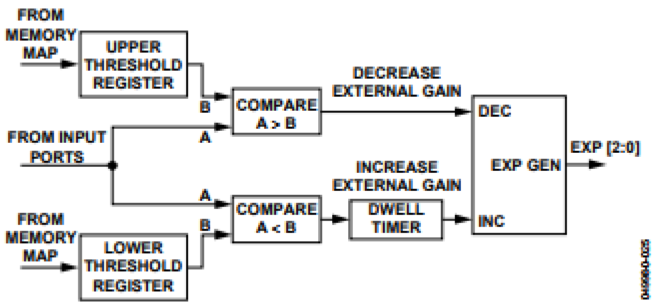


Figure 25. AD6636 Gain Control Block Diagram

ADC INPUT PORT MONITOR FUNCTION

The AD6636 provides a power-monitor function that can monitor and gather statistics about the received signal in a signal chain. Each input port is equipped with an individual power-monitor function that can operate both in real and complex modes of the input port. This function block can operate in one of three modes, which measure the following over a programmable period of time:

- Peak power
- Mean power
- Number of samples crossing a threshold

These functions are controlled via the 2-bit power-monitor function select bits of the power monitor control register for each individual input port. The input ports can be set for different modes, but only one function can be active at a time for any given input port.

The three modes of operation can function continuously over a programmable time period. This time period is programmed as the number of input clock cycles in a 24-bit ADC monitor period register (AMPR). This register is separate for each input port. An internal magnitude storage register (MSR) is used to monitor, accumulate, or count, depending on the mode of operation.

Peak Detector Mode (Control Bits 00)

The magnitude of the input port signal is monitored over a programmable time period (given by AMPR) to give the peak value detected. This mode is set by programming Logic 0 in the power-monitor function select bits of the power-monitor control register for each individual input port. The 24-bit AMPR must be programmed before activating this mode.

After enabling this mode, the value in the AMPR is loaded into a monitor period timer and the countdown is started. The magnitude of the input signal is compared to the MSR, and the greater of the two is updated back into the MSR. The initial value of the MSR is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the MSR is transferred to the power-monitor holding register, which can be read through the microport or the serial port. The monitor period timer is reloaded with the value in the AMPR, and the countdown is started. Also, the first input sample's magnitude is updated in the MSR, and the comparison and update procedure, as explained above, continues. If the interrupt is enabled, an interrupt is generated, and the interrupt status register is updated when the AMPR reaches a count of 1.

Figure 26 is a block diagram of the peak detector logic. The MSR contains the absolute magnitude of the peak detected by the peak detector logic.

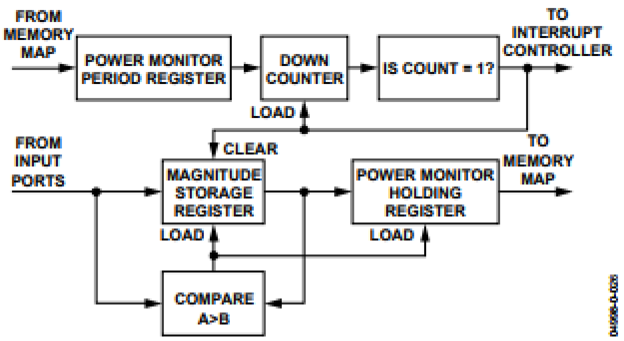


Figure 26. ADC Input Peak Detector Block Diagram

Mean Power Mode (Control Bits 01)

In this mode, the mean power of the input port signal is integrated (by adding an accumulator) over a programmable time period (given by AMPR) to give the mean power of the input signal. This mode is set by programming Logic 1 in the power monitor function select bits of the power monitor control register for each individual input port. The 24-bit AMPR, representing the period over which integration is performed, must be programmed before activating this mode.

After enabling this mode, the value in the AMPR is loaded into a monitor period timer, and the countdown is started immediately. The 15-bit mean power of input signal is right-shifted by nine bits to give 6-bit data. This 6-bit data is added to the contents of a 24-bit holding register, thus performing an accumulation. The integration continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the MSR is transferred to the power-monitor holding register (after some formatting), which can be read through the microport or the serial port. The monitor period timer is reloaded with the value in the AMPR, and the countdown is started. Also, the first input sample signal power is updated in the MSR, and the accumulation continues with the subsequent input samples. If the interrupt is enabled, an interrupt is generated, and the interrupt status register is updated when the AMPR reaches a count of 1. Figure 27 illustrates the mean power-monitoring logic.

The value in the MSR is a floating-point number with 4 MSBs and 20 LSBs. If the 4 MSBs are EXP and the 20 LSBs are MAG, the value in dBFS can be decoded by

$$Mean\ Power = 10\log\left[\left(\frac{MAG}{2^{20}}\right)2^{-(EXP-1)}\right]$$

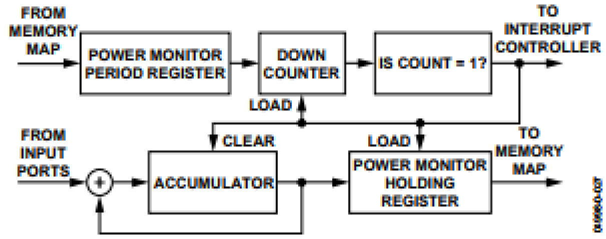


Figure 27. ADC Input Mean Power-Monitoring Block Diagram

Threshold Crossing Mode (Control Bits 10)

In this mode of operation, the magnitude of the input port signal is monitored over a programmable time period (given by AMPR) to count the number of times it crosses a certain programmable threshold value. This mode is set by programming Logic 1x (where x is a don't care bit) in the power-monitor function select bits of the power monitor control register for each individual input port. Before activating this mode, the user needs to program the 24-bit AMPR and the 10-bit upper threshold register for each individual input port. The same upper threshold register is used for both power monitoring and gain control (see the ADC Gain Control section).

After entering this mode, the value in the AMPR is loaded into a monitor period timer, and the countdown is started. The magnitude of the input signal is compared to the upper threshold register (programmed previously) on each input clock cycle. If the input signal has magnitude greater than the upper threshold register, then the MSR register is incremented by 1. The initial value of the MSR is set to 0. This comparison and increment of the MSR register continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the MSR is transferred to the power monitor holding register, which can be read through the microport or the serial port. The monitor period timer is reloaded with the value in the AMPR, and the countdown is started. The MSR register is also cleared to a value of 0. If interrupts are enabled, an interrupt is generated, and the interrupt status register is updated when the AMPR reaches a count of 1. Figure 28 illustrates the threshold crossing logic. The value in the MSR is the number of samples that have an amplitude greater than the threshold register.

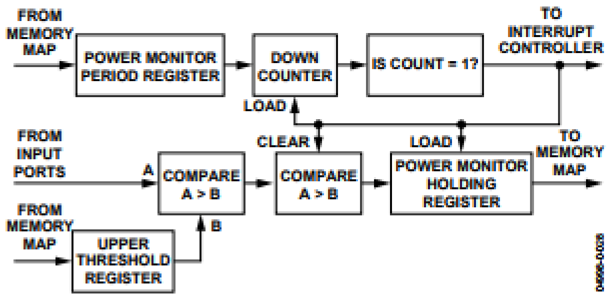


Figure 28. ADC Input Threshold Crossing Block Diagram

Additional Control Bits

For additional flexibility in the power monitoring process, two control bits are provided in the power-monitor control register. They are the disable monitor period timer bit and the clear-on-read bit. These options have the same function in all three modes of operation.

Disable Monitor Period Timer Bit

When the disable monitor period timer bit is written with Logic 1, the timer continues to run but does not cause the contents of the MSR to be transferred to the holding register when the count reaches 1. This function of transferring the MSR to the power monitor holding register and resetting the MSR is now controlled by a read operation on the microport or serial port.

When a microport or serial port read is performed on the power monitor holding register, the MSR value is transferred to the holding register. After the read operation, the timer is reloaded with the AMPR value. If the timer reaches 1 before the microport or serial port read, the MSR value is not transferred to the holding register, as in normal operation. The timer still generates an interrupt on the AD6636 interrupt pin and updates the interrupt status register. An interrupt appears on the $\overline{IRP}$ pin, if interrupts are enabled in the interrupt enable register.

Clear-on-Read Bit

This control bit is valid when the disable monitor period timer bit is Logic 1 only. When both of these bits are set, a read operation to either the microport or the serial port reads the MSR value, and the monitor period timer is reloaded with the AMPR value. The MSR is cleared (written with current input signal magnitude in peak power and mean power mode; written with a 0 in threshold crossing mode), and normal operation continues.

When the monitor period timer is disabled and the clear-on-read bit is set, a read operation to the power monitor holding register clears the contents of the MSR and, therefore, the power monitor loop restarts.

If the clear-on-read bit is Logic 0, the read operation to the microport or serial port does not clear the MSR value after it is transferred into the holding register. The value from the previous monitor time period persists, and it continues to be compared, accumulated, or incremented, based on new input signal magnitude values.

QUADRATURE I/Q CORRECTION BLOCK

When the I and Q paths are digitized using separate ADCs, as in quadrature IF down-conversion, a mismatch often occurs between I and Q due to variations in the ADCs from the manufacturing process. The AD6636 is equipped with two quadrature correction blocks that can be used to correct I/Q mismatch errors in a complex baseband input stream. These I/Q mismatches can result in spectral distortions and removing them is useful.

Two such blocks are present, one each for the I/Q signal formed by combining the A and B inputs and the C and D inputs, respectively. The I/Q correction block can be enabled when the Port A (or Port C) complex data active bit is enabled in the ADC input control register. This block is bypassed when real input data is present on the ADC input ports because there is no possibility of I/Q mismatch in real data.

The I/Q or quadrature correction block consists of three independent subblocks: dc correction, phase correction, and amplitude correction. Three individual bits in the AB (or CD) correction control registers can be used to enable or disable each of these subblocks independently. Figure 29 shows the contents and definitions of the registers related to the quadrature correction block.

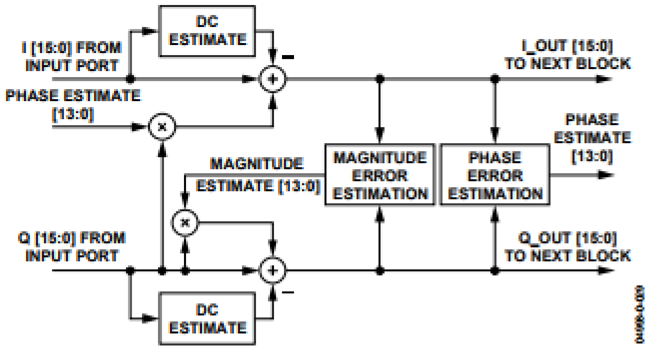


Figure 29. Quadrature Correction Block Diagram

Table 12. Correction Control Registers

Register	Bits	Description
I/Q Correction Control	15 to 12	Amplitude Loop BW
	11 to 8	Phase Loop BW
	7 to 4	DC Loop BW
	3	Reserved (Logic 0)
	2	Amplitude Correction Enable
	1	Phase Correction Enable
	0	DC Correction Enable
DC Offset Correction I	31 to 16	DC Offset Q
DC Offset Correction Q	15 to 0	DC Offset I
Amplitude Offset Correction	31 to 16	Amplitude Correction
Phase Offset Correction	15 to 0	Phase Correction

DC Correction

All ADCs have a nominal dc offset related to them. If the ADCs in the I and Q path have different dc offsets due to variations in the manufacturing process, the dc correction circuit can be used to compensate for these dc offsets. Writing Logic 1 into the dc correction enable bit of the AB (or CD) correction control register enables the dc correction block. Two dc estimation blocks are used, one each for the I and Q paths. The estimated dc value is subtracted from the I and Q paths. Therefore, the dc signal is removed independently from the I and Q path signals.

A cascade of two low-pass decimating filters estimates the dc offset in the feedback loop. A decimating first-order CIC filter is followed by an interpolating second-order CIC filter. The decimation and interpolation values of the CIC filters are the same and are programmable between 2^{12} and 2^{24} in powers of 2.

The 4-bit dc loop BW word in the I/Q correction control AB (or CD) register is used to program this decimation (interpolation) value. When the dc loop BW is a 0, decimation is 2^{12}, and when the dc loop BW is 11, decimation is 2^{24}.

When the dc correction circuit is enabled, the dc correction values are estimated. The values, which are estimated independently in the I and Q paths, are subtracted independently from their respective datapaths. These dc correction values are also available for output continuously through the dc correction I and dc correction Q registers. These registers contain 16-bit dc offset values whose MSB-justified values are subtracted directly from MSB-justified ADC inputs for the I and Q paths.

When the dc correction circuit is disabled, the value in the dc correction register is used for continuously subtracting the dc offset from I and Q datapaths. This method can be used to manually set the dc offset instead of using the automatic dc correction circuit.

Phase Correction

When using complex ADC input, the I and Q datapaths typically have phase offset, caused mainly by the local oscillator and demodulator IC. The AD6636 phase-offset correction circuit can be used to compensate for this phase offset.

When the phase correction enable bit is Logic 1, the phase error between I and Q is estimated (ideally, the phase should be 90°). The phase mismatch is estimated over a period of time determined by the integrator loop bandwidth. This integrator is implemented as a first-order CIC decimating filter, whose decimation value can vary between 2^{12} and 2^{24} in powers of 2. Phase loop BW (Bits [11:8]) of the I/Q correction control register determine this decimation value. When phase loop BW equals 0, the decimation value is 2^{12}, and when phase loop BW is 11, the decimation value is 2^{24}.

While the phase offset correction circuit is enabled, the tan(phase_mismatch) is estimated continuously. This value is multiplied with Q path data and added to I path data continuously. The estimated value is also updated in the phase offset correction register. The tan(phase_mismatch) can be ±0.125 with a 14-bit resolution. This converts to a phase mismatch of about ±7.125°.

When the phase offset correction circuit is disabled, the value in the phase correction register is multiplied by the Q path data and added to the I path data continuously. This method can be used to manually set the phase offset instead of using the automatic phase offset correction circuit.

Amplitude Correction

When using complex ADC input, the I and Q datapaths typically have amplitude offset, caused mainly by the local oscillator and the demodulator IC. The AD6636 amplitude offset correction circuit can be used to compensate for this amplitude offset.

When the amplitude correction enable bit is Logic 1, the amplitude error between the I and Q datapaths is estimated. The amplitude mismatch is estimated over a period of time determined by the integrator loop bandwidth. This integrator is implemented as a first-order CIC decimating filter, whose decimation value can vary between 2^{12} and 2^{24} in powers of 2. Phase loop BW (Bits [11:8]) of the I/Q correction control register determines this decimation value. When the phase loop BW equals 0, the decimation value is 2^{12}, and when phase loop BW is 11, the decimation value is 2^{24}.

While the amplitude offset correction circuit is enabled, the difference (MAG(Q) − MAG(I)) is estimated continuously. This value is multiplied with the Q path data and added to the Q path data continuously. The estimated value is also updated in the phase offset correction register. The difference (MAG(Q) −

MAG(I)) can be between 1.125 and 0.875 with a 14-bit resolution.

When the amplitude offset correction circuit is disabled, the value in the amplitude offset correction register is multiplied by the Q path data and added to the Q path data continuously. This method can be used to manually set the amplitude offset instead of using the automatic amplitude offset correction circuit.

INPUT CROSSBAR MATRIX

The AD6636 has four ADC input ports and six channels. Two input ports can be paired to support complex input ports. Crossbar mux selection allows each channel to select its input signal from the following sources: four real input ports, two complex input ports, and internally generated pseudorandom sequence (referred to as a PN sequence, which can be either real or complex). Each channel has an input crossbar matrix to select from the above-listed input signal choices.

The selection of the input signal for a particular channel is made using a 3-bit crossbar mux select word and a 1-bit complex data input bit selection in the ADC input control register. Each channel has a separate selection for individual control. Table 13 lists the valid combinations of the crossbar mux select word, the complex data input bit values, and the corresponding input signal selections.

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

Each channel consists of an independent complex NCO and a complex mixer. This processing stage has a digital tuner consisting of three multipliers and a 32-bit complex NCO. The NCO serves as a quadrature local oscillator capable of producing an NCO frequency of between −CLK/2 and +CLK/2 with a resolution of $CLK/2^{32}$ in complex mode, where CLK is the input clock frequency.

The frequency word used for generating the NCO is a 32-bit word. This word is used to generate a 20-bit phase word. A 16-bit phase offset word is added to this phase word. Eighteen bits of this phase word are used to generate the sine and cosine of the required NCO frequency.

The amplitude of the sine and cosine are represented using 17 bits. The worst-case spurious signal from the NCO is better than −100 dBc for all output frequencies.

Because the filtering in the AD6636 is low-pass filtering, the carrier of interest is tuned down to dc (frequency = 0 Hz). This is illustrated in Figure 30. Once the signal of interest is tuned down to dc, the unwanted adjacent carriers can be rejected using the low-pass filtering that follows.

NCO Frequency

The NCO frequency value is given by the 32-bit twos complement number entered in the NCO frequency register. Frequencies between −CLK/2 and CLK/2 (CLK/2 excluded) are represented using this frequency word:

0x8000 0000 represents a frequency given by −CLK/2.

0x0000 0000 represents dc (frequency is 0 Hz).

0x7FFF FFFF represents $CLK/2 - CLK/2^{32}$.

The NCO frequency word can be calculated by

$$NCO\_FREQ = 2^{32}\frac{\mathrm{mod}(f_{ch}, f_{clk})}{f_{clk}}$$

where:

NCO_FREQ is the 32-bit twos complement number representing the NCO frequency register.

f_{ch} is the desired carrier frequency.

f_{clk} is the clock rate for the channel under consideration.

mod( ) is a remainder function. For example, mod(110, 100) = 10 and, for negative numbers, mod(−32, 10) = −2.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

Table 13. Crossbar Mux Selection for Channel Input Signal

Complex Input Bit	Crossbar Mux Select Bit	Input Signal Selection
0	000	Input Port A magnitude and exponent pins drive the channel.
0	001	Input Port B magnitude and exponent pins drive the channel.
0	010	Input Port C magnitude and exponent pins drive the channel.
0	011	Input Port D magnitude and exponent pins drive the channel.
0	100	Internal PN sequence's magnitude and exponent bits drive the channel.
1	000	Input Ports A and B form a pair to drive I and Q paths of the channel, respectively. Input Port A exponent pins drive the channel exponent bits.
1	001	Input Ports C and D form a pair to drive I and Q paths of the channel, respectively. Input Port C exponent pins drive the channel exponent bits.
1	010	Internal PN sequence's magnitude and exponent bits drive the channel.