INMOS CORP

IMS1403

CMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 1 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

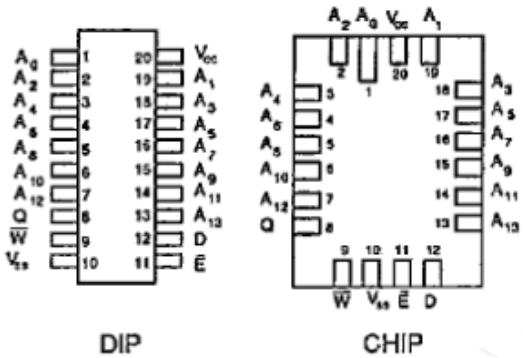
DESCRIPTION

The INMOS IMS1403 is a high performance 16K x 1 CMOS Static RAM. The IMS1403 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

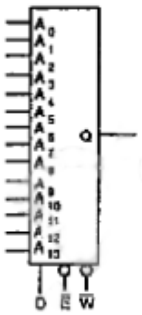
The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1403M and IMS1403LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM

PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q .....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		75	mA	t_{AVAV} = t_{AVAV} (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\bar{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E}$ ≥ (Vcc - 0.2). All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E}$ ≥ (Vcc - 0.2). Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 16mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.