Dual Bidirectional I²C Bus and SMBus Repeater

1 Features

- Two-Channel Bidirectional Buffers
- I²C Bus and SMBus Compatible
- Active-High Repeater-Enable Input
- Open-Drain I²C I/O
- 5.5-V Tolerant I²C I/O and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters
- Powered-Off High-Impedance I²C Pins
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This dual bidirectional I²C buffer is operational at 2.3-V to 3.6-V V_{CC}.

The PCA9515A is a BiCMOS integrated circuit intended for I²C bus and SMBus systems applications. The device contains two identical bidirectional open-drain buffer circuits that enable I²C and similar bus systems to be extended without degradation of system performance.

The PCA9515A buffers both the serial data (SDA) and serial clock (SCL) signals on the I²C bus, while retaining all the operating modes and features of the I²C system. This enables two buses of 400-pF bus capacitance to be connected in an I²C application.

The I²C bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515A enables the system designer to isolate two halves of a bus, accommodating more I²C devices or longer trace lengths.

The PCA9515A has an active-high enable (EN) input with an internal pullup, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It never should change state during an I²C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I²C parts being enabled. The EN input should change state only when the global bus and the repeater port are in an idle state, to prevent system failures.

The PCA9515A also can be used to run two buses: one at 5-V interface levels and the other at 3.3-V interface levels, or one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz, because of the delays that are added by the repeater.

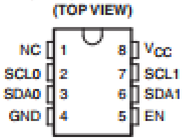
The PCA9515A does not support clock stretching across the repeater.

Device Information[(1)]

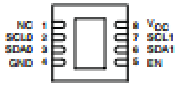
PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9515A	SOIC (8)	4.90 mm × 3.91 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

D, DCT, DGK, OR PW PACKAGE
(TOP VIEW)



DRG PACKAGE
(TOP VIEW)



NC – No internal connection

4 Description (Continued)

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lockup condition from occurring when the input low condition is released.

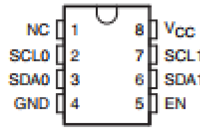
Two or more PCA9515A devices cannot be used in series. The PCA9515A design does not allow this configuration. Because there is no direction pin, slightly different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low applied at the input of a PCA9515A is propagated as a buffered low with a slightly higher value on the enabled outputs. When this buffered low is applied to another PCA9515A-type device in series, the second device does not recognize it as a valid low and does not propagate it as a buffered low again.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until V_{CC} is at a valid level (V_{CC} = 2.3 V).

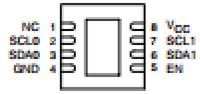
As with the standard I²C system, pullup resistors are required to provide the logic high levels on the buffered bus. The PCA9515A has standard open-collector configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I²C devices in addition to SMBus devices. Standard Mode I²C devices only specify 3 mA in a generic I²C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

5 Pin Configuration and Functions

D, DCT, DGK, OR PW PACKAGE
(TOP VIEW)



DRG PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NC	1	No internal connection
SCL0	2	Serial clock bus 0
SDA0	3	Serial data bus 0
GND	4	Supply ground
EN	5	Active-high repeater enable input
SDA1	6	Serial data bus 1
SCL1	7	Serial clock bus 1
V_{CC}	8	Supply power

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range[2]		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range[2]		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[3]	D package		97	°C/W
		DCT package		220	
		DGK package		172	
		DRG package		TBD	
		PW package		149	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	SDA and SCL inputs	$0.7 \times V_{CC}$	5.5	V
		EN input	2	5.5	
V_{IL}[1]	Low-level input voltage	SDA and SCL inputs	–0.5	$0.3 \times V_{CC}$	V
		EN input	–0.5	0.8	
V_{ILc}[1]	SDA and SCL low-level input voltage contention		–0.5	0.4	V
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 3 V		6	
T_A	Operating free-air temperature		–40	85	°C

(1) V_{IL} specification is for the EN input and the first low level seen by the SDAx and SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx and SCLx lines. V_{ILc} must be at least 70 mV below V_{OL}.

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18 mA	2.3 V to 3.6 V			–1.2	V
V_{OL}	Low-level output voltage	SDAx, SCLx	I_{OL} = 20 µA or 6 mA	2.3 V to 3.6 V	0.47	0.52	0.6	V
$V_{OL} - V_{ILc}$	Low-level input voltage below low-level output voltage	SDAx, SCLx	I_I = 10 µA	2.3 V to 3.6 V			70	mV
I_{CC}	Quiescent supply current		Both channels high, SDAx = SCLx = V_{CC}	2.7 V		0.5	3	mA
				3.6 V		0.5	3	
			Both channels low, SDA0 = SCL0 = GND and SDA1 = SCL1 = open; or SDA0 = SCL0 = open and SDA1 = SCL1 = GND	2.7 V		1	4	
				3.6 V		1	4	
			In contention, SDAx = SCLx = GND	2.7 V		1	4	
				3.6 V		1	4	
I_I	Input current	SDAx, SCLx	V_I = 3.6 V	2.3 V to 3.6 V			±1	µA
			V_I = 0.2 V				3	
		EN	V_I = V_{CC}				±1	
			V_I = 0.2 V			–10	–20	
I_{off}	Leakage current	SDAx, SCLx	V_I = 3.6 V, EN = L or H	0 V			0.5	µA
			V_I = GND, EN = L or H				0.5	
$I_{I(ramp)}$	Leakage current during power up	SDAx, SCLx	V_I = 3.6 V, EN = L or H	0 V to 2.3 V			1	µA
C_{in}	Input capacitance	EN	V_I = 3 V or GND	3.3 V		7	9	pF
		SDAx, SCLx	V_I = 3 V or GND, EN = H	3.3 V		7	9	

(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and T_A = 25°C.

6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{su}	Setup time, EN↑ before Start condition	100		100		ns
t_h	Hold time, EN↓ after Stop condition	130		100		ns

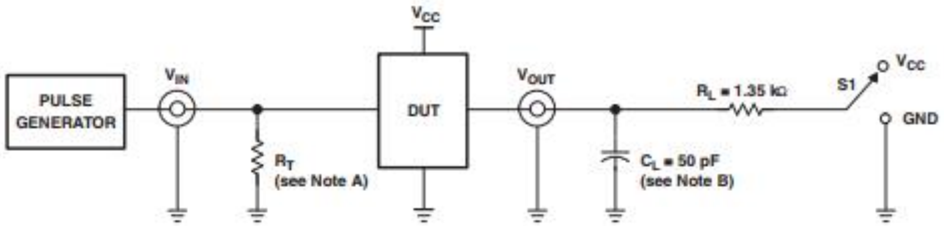
6.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L \le 100$ pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			V_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PZL}	Propagation delay time[2]	SDA0, SCL0 or SDA1, SCL1	SDA1, SCL1 or SDA0, SCL0	45	82	130	45	68	120	ns
t_{PLZ}				33	113	190	33	102	180	
t_{THL}	Output transition time[2] (SDAx, SCLx)	80%	20%		57			58		ns
t_{TLH}		20%	80%		148			147		

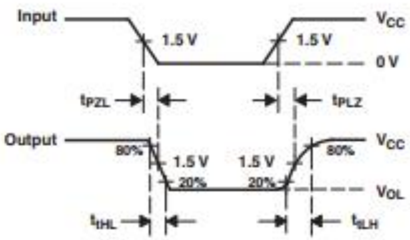
(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and T_A = 25°C.
(2) Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.

7 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

G. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

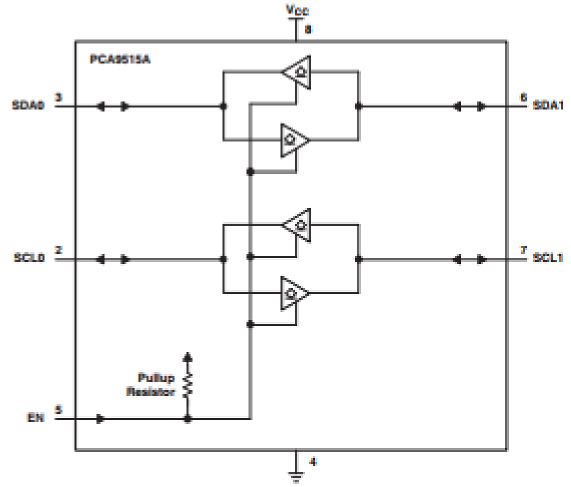


Figure 2. Logic Diagram (Positive Logic)

8.2 Feature Description

8.2.1 Clock Stretching Errata

Description

Due to the static offset on both sides of the buffer (SCLx & SDAx) and the possibility of an overshoot above 500 mV during events like clock stretching, the device should not be used with rise time accelerators.

System Impact

An incorrect logic state will be passed through the buffer, creating an I2C communication failure on the bus.

System Workaround

There is a possible workaround to avoid an I2C communication failure:

- Do not use rise-time accelerators in conjunction with the PCA9515A.

8.3 Device Functional Modes

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDA0 = SDA1 SCL0 = SCL1

9 Application and Implementation

9.1 Typical Application

A typical application is shown in Figure 3. In this example, the system master is running on a 3.3-V bus, while the slave is connected to a 5-V bus. Both buses run at 100 kHz, unless the slave bus is isolated, and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

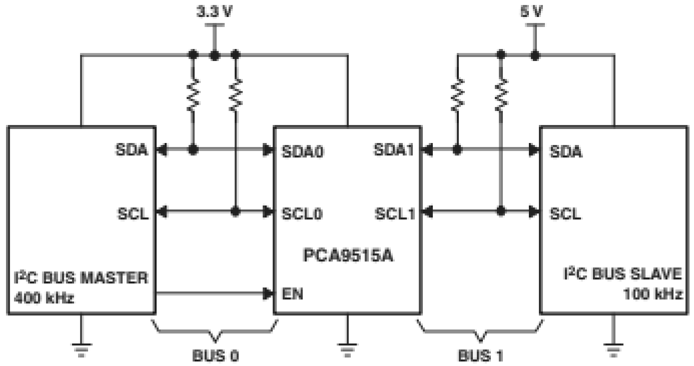


Figure 3. Typical Application

9.1.1 Design Requirements

The PCA9515A is 5.5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515A is pulled low by a device on the I²C bus, a CMOS hysteresis-type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side also to go low. The side driven low by the PCA9515A typically is at V_{OL} = 0.5 V.

9.1.2 Detailed Design Procedure

Figure 4 and Figure 5 show the waveforms that are seen in a typical application. If the bus master in Figure 3 writes to the slave through the PCA9515A, Bus 0 has the waveform shown in Figure 4. This looks like a normal I²C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515A. Because the V_{OL} of the PCA9515A typically is around 0.5 V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

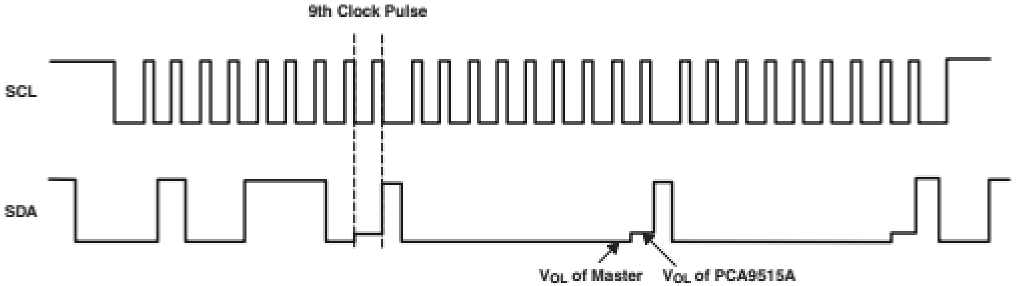


Figure 4. Bus 0 Waveforms

Typical Application (continued)

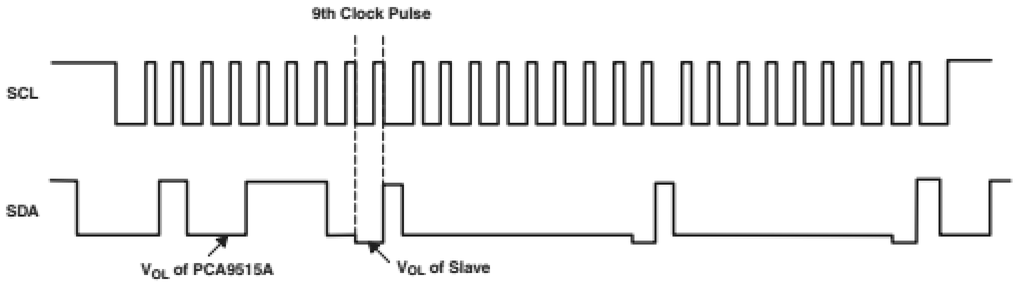


Figure 5. Bus 1 Waveforms

On the Bus 1 side of the PCA9515A, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PCA9515A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in the example.

10 Device and Documentation Support

10.1 Trademarks

All trademarks are the property of their respective owners.

10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.