1 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer

Data Sheet **AD9910**

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz analog output)
- Integrated 1 GSPS, 14-bit DAC
- 0.23 Hz or better frequency resolution
- Phase noise ≤ −125 dBc/Hz @ 1 kHz offset (400 MHz carrier)
- Excellent dynamic performance with
  - >80 dB narrow-band SFDR
- Serial input/output (I/O) control
- Automatic linear or arbitrary frequency, phase, and amplitude sweep capability
- 8 frequency and phase offset profiles
- Sin(x)/(x) correction (inverse sinc filter)
- 1.8 V and 3.3 V power supplies
- Software and hardware controlled power-down
- 100-lead TQFP_EP package
- Integrated 1024 word × 32-bit RAM
- PLL REFCLK multiplier
- Parallel datapath interface
- Internal oscillator can be driven by a single crystal
- Phase modulation capability
- Amplitude modulation capability
- Multichip synchronization

APPLICATIONS

- Agile local oscillator (LO) frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulators
- Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

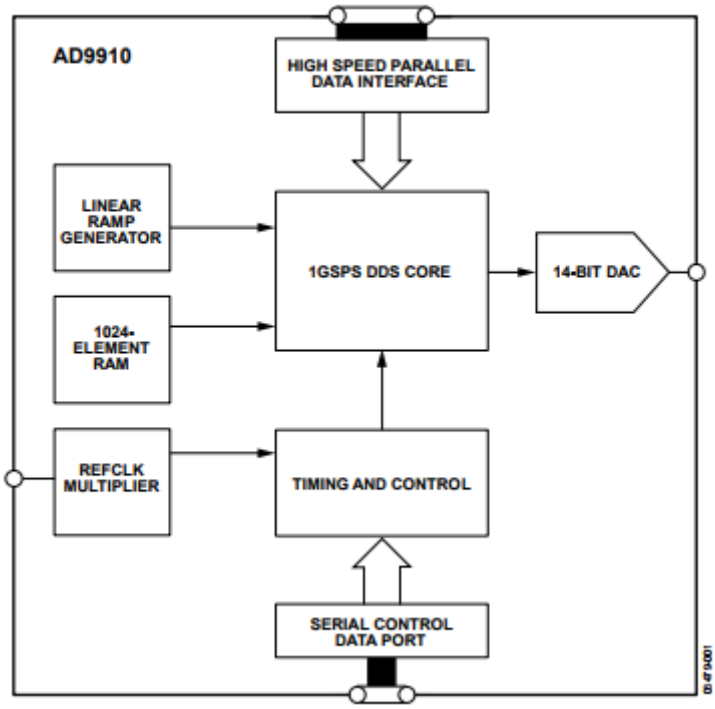


Figure 1.

GENERAL DESCRIPTION

The AD9910 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS. The AD9910 employs an advanced, proprietary DDS technology that provides a significant reduction in power consumption without sacrificing performance. The DDS/DAC combination forms a digitally programmable, high frequency, analog output synthesizer capable of generating a frequency agile sinusoidal waveform at frequencies up to 400 MHz.

The user has access to the three signal control parameters that control the DDS: frequency, phase, and amplitude. The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1 GSPS sample rate, the tuning resolution is ~0.23 Hz. The DDS also enables fast phase and amplitude switching capability.

The AD9910 is controlled by programming its internal control registers via a serial I/O port. The AD9910 includes an integrated static RAM to support various combinations of frequency, phase, and/or amplitude modulation. The AD9910 also supports a user defined, digitally controlled, digital ramp mode of operation. In this mode, the frequency, phase, or amplitude can be varied linearly over time. For more advanced modulation functions, a high speed parallel data input port is included to enable direct frequency, phase, amplitude, or polar modulation.

The AD9910 is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section for details).

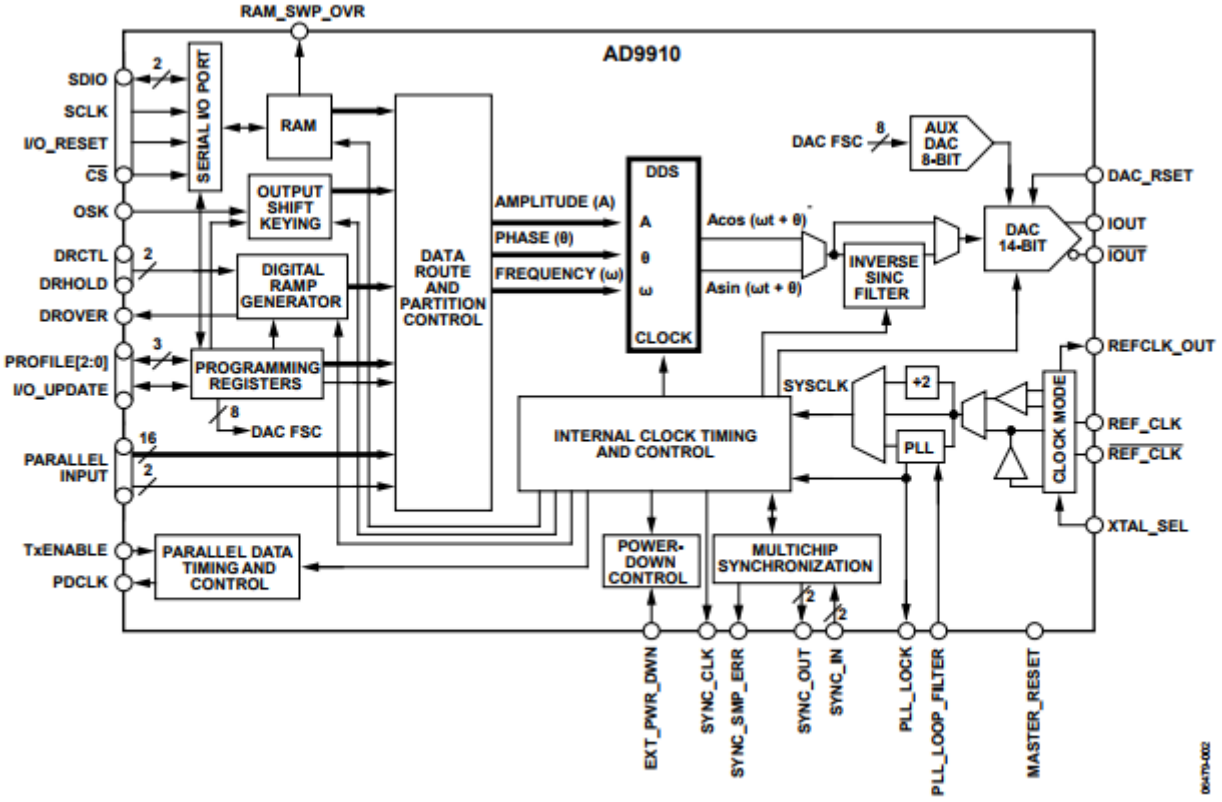


Figure 2. Detailed Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) = 3.3 V ± 5%, DVDD_I/O (3.3 V) = 3.3 V ± 5%, T = 25°C, R_{SET} = 10 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with reference clock (REFCLK) multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
REFCLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3		pF
Input Impedance	Differential		2.8		kΩ
	Single-ended		1.4		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REFCLK Input Level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO CHARACTERISTICS					
VCO Gain (K_V) @ Center Frequency	VCO range Setting 0		429		MHz/V
	VCO range Setting 1		500		MHz/V
	VCO range Setting 2		555		MHz/V
	VCO range Setting 3		750		MHz/V
	VCO range Setting 4		789		MHz/V
	VCO range Setting 5[1]		850		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			20		pF
Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.6	20	31.6	mA
Gain Error		−10		+10	% FS
Output Offset				2.3	µA
Differential Nonlinearity			0.8		LSB
Integral Nonlinearity			1.5		LSB
Output Capacitance			5		pF
Residual Phase Noise	@ 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		−152		dBc/Hz
	Enabled @ 20×		−140		dBc/Hz
	Enabled @ 100×		−140		dBc/Hz
Voltage Compliance Range		−0.5		+0.5	V
Wideband SFDR	See the Typical Performance Characteristics section				
Narrow-Band SFDR					
50.1 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−96		dBc
101.3 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−95		dBc

Parameter	Conditions/Comments	Min	Typ	Max	Unit
201.1 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−91		dBc
301.1 MHz Analog Output	±500 kHz		−86		dBc
	±125 kHz		−86		dBc
	±12.5 kHz		−88		dBc
401.3 MHz Analog Output	±500 kHz		−84		dBc
	±125 kHz		−84		dBc
	±12.5 kHz		−85		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Clock Pulse Width	Low	4			ns
	High	4			ns
Maximum SCLK Rise/Fall Time			2		ns
Minimum Data Setup Time to SCLK		5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PROFILE[2:0] TIMING CHARACTERISTICS					
Minimum Setup Time to SYNC_CLK		1.75			ns
Minimum Hold Time to SYNC_CLK		0			ns
I/O_UPDATE Pulse Width	High	>1			SYNC_CLK cycle
Minimum Profile Toggle Period		2			SYNC_CLK cycles
TxENABLE and 16-BIT PARALLEL (DATA) BUS TIMING					
Maximum PDCLK Frequency			250		MHz
TxENABLE/Data Setup Time (to PDCLK)		1.75			ns
TxENABLE/Data Hold Time (to PDCLK)		0			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[2]					
Fast Recovery			8		SYSCLK cycles[3]
Full Sleep Mode	REFCLK multiplier enabled		1		ms
	REFCLK multiplier disabled			150	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[3]
DATA LATENCY (PIPELINE DELAY)					
Data Latency, Single Tone or Using Profiles					
Frequency, Phase, Amplitude-to-DAC Output	Matched latency enabled and OSK enabled		91		SYSCLK cycles[3]
Frequency, Phase-to-DAC Output	Matched latency enabled and OSK disabled		79		SYSCLK cycles[3]
	Matched latency disabled		79		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency Using RAM Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		94		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		106		SYSCLK cycles[3]
	Matched latency disabled		58		SYSCLK cycles[3]
Data Latency, Sweep Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		91		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles[3]
	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency, 16-Bit Input Modulation Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled		103		SYSCLK cycles[3]
	Matched latency disabled		91		SYSCLK cycles[3]

Parameter	Conditions/Comments	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
Logic 1 Voltage		2.0			V
Logic 0 Voltage				0.8	V
Logic 1 Current			90	150	µA
Logic 0 Current			90	150	µA
Input Capacitance			2		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V
Input Capacitance			2		pF
CMOS LOGIC OUTPUTS	1 mA load				
Logic 1 Voltage		2.8			V
Logic 0 Voltage				0.4	V
POWER SUPPLY CURRENT					
I_{AVDD} (1.8 V)			110		mA
I_{AVDD} (3.3 V)			29		mA
I_{DVDD} (1.8 V)			222		mA
I_{DVDD} (3.3 V)			11		mA
TOTAL POWER CONSUMPTION					
Single Tone Mode			715	950	mW
Rapid Power-Down Mode			330	450	mW
Full Sleep Mode			19	40	mW

[1] The gain value for VCO range Setting 5 is measured at 1000 MHz.
[2] Wake-up time refers to the recovery time from a power-down state. The longest time required is for the reference clock multiplier PLL to relock to the reference. The wake-up time assumes that the recommended PLL loop filter values are used.
[3] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external reference clock frequency.

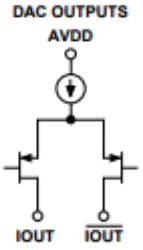
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVDD (1.8V), DVDD (1.8V) Supplies	2 V
AVDD (3.3V), DVDD_I/O (3.3V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
XTAL_SEL	−0.7 V TO +2.2 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
θ_{JA}	22°C/W
θ_{JC}	2.8°C/W
Maximum Junction Temperature	150°C
Lead Temperature (10 sec Soldering)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

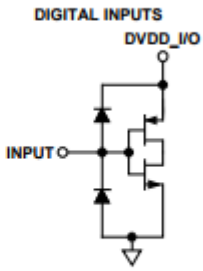
EQUIVALENT CIRCUITS



MUST TERMINATE OUTPUTS TO AGND FOR CURRENT FLOW. DO NOT EXCEED THE OUTPUT VOLTAGE COMPLIANCE RATING.

06479-003

Figure 3. Equivalent Input Circuit

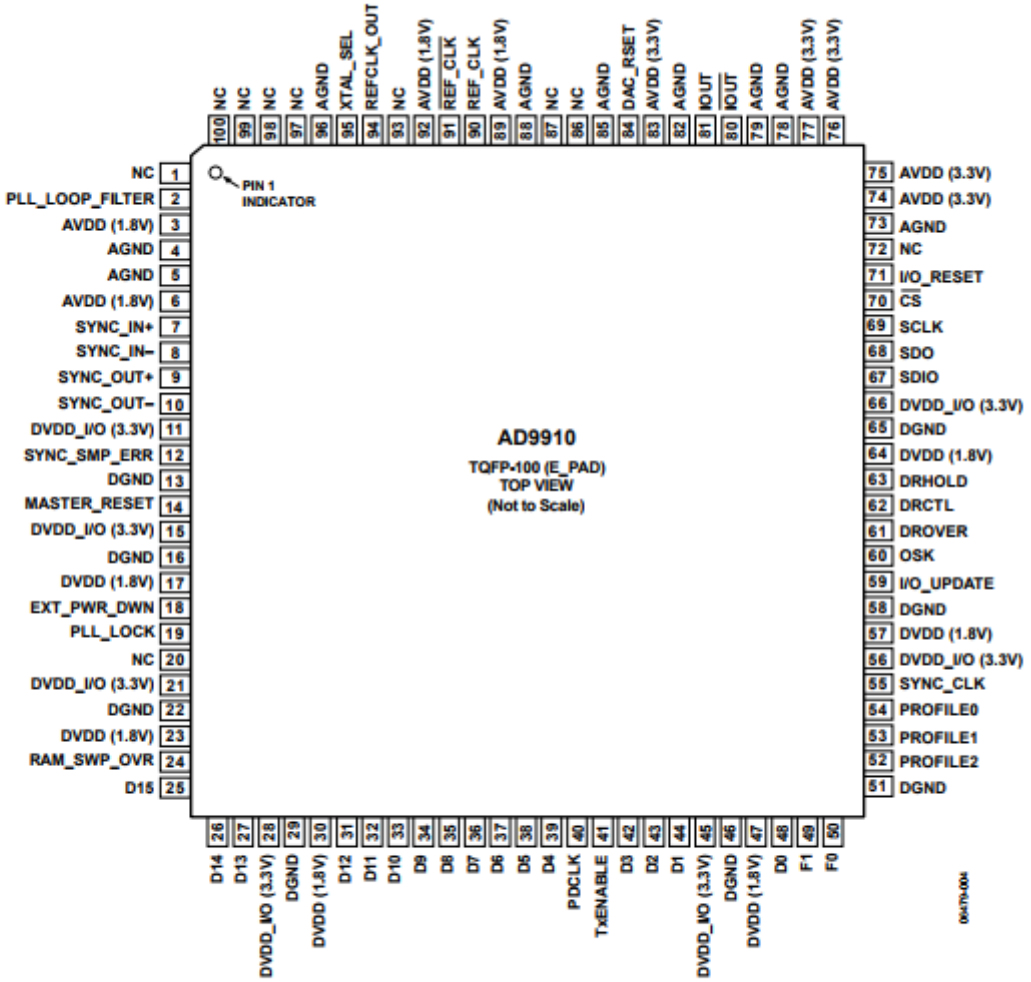


AVOID OVERDRIVING DIGITAL INPUTS. FORWARD BIASING ESD DIODES MAY COUPLE DIGITAL NOISE ONTO POWER PINS.

06479-005

Figure 4. Equivalent Output Circuit

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES:
1. EXPOSED PAD SHOULD BE SOLDERED TO GROUND.
2. NC = NO CONNECT.

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 20, 72, 86, 87, 93, 97 to 100	NC		Not Connected. Allow device pins to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation Pin. See the External PLL Loop Filter Components section for details.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD, 1.8 V Analog Supplies.
74 to 77, 83	AVDD (3.3V)	I	Analog DAC VDD, 3.3 V Analog Supplies.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD, 1.8 V Digital Supplies.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD, 3.3 V Digital Supplies.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 51, 58, 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal (LVDS), Digital Input (Rising Edge Active). The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
8	SYNC_IN–	I	Synchronization Signal (LVDS), Digital Input. The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
9	SYNC_OUT+	O	Synchronization Signal (LVDS), Digital Output (Rising Edge Active). The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
10	SYNC_OUT–	O	Synchronization Signal (LVDS), Digital Output. The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). Sync sample error: a high on this pin indicates that the AD9910 did not receive a valid sync signal on SYNC_IN+/SYNC_IN–.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section for further details. If unused, connect to ground.
19	PLL_LOCK	O	Clock Multiplier PLL Lock, Digital Output (Active High). A high on this pin indicates that the Clock Multiplier PLL has acquired lock to the reference clock input.
24	RAM_SWP_OVR	O	RAM Sweep Over, Digital Output (Active High). A high on this pin indicates that the RAM sweep profile has completed.
25 to 27, 31 to 39, 42 to 44, 48	D[15:0]	I	Parallel Input Bus (Active High).
49, 50	F[1:0]	I	Modulation Format Pins. Digital input to determine the modulation format.
40	PDCLK	O	Parallel Data Clock. This is the digital output (clock). The parallel data clock provides a timing signal for aligning data at the parallel inputs.
41	TxENABLE	I	Transmit Enable. Digital input (active high). In burst mode communications, a high on this pin indicates new data for transmission. In continuous mode, this pin remains high.
52 to 54	PROFILE[2:0]	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. State changes should be set up on the SYNC_CLK pin.
55	SYNC_CLK	O	Output Clock Divided-By-Four. A digital output (clock). Many of the digital inputs on the chip, such as I/O_UPDATE and PROFILE[2:0], need to be set up on the rising edge of this signal.

Pin No.	Mnemonic	I/O[1]	Description
59	I/O_UPDATE	I/O	Input/Output Update. Digital input (active high). A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero, a high sweeps the amplitude up to the amplitude scale factor.
61	DROVER	O	Digital Ramp Over. Digital output (active high). This pin switches to Logic 1 whenever the digital ramp generator reaches its programmed upper or lower limit.
62	DRCTL	I	Digital Ramp Control. Digital input (active high). This pin controls the slope polarity of the digital ramp generator. See the Digital Ramp Generator (DRG) section for more details. If not using the digital ramp generator, connect this pin to Logic 0.
63	DRHOLD	I	Digital Ramp Hold. Digital input (active high). This pin stalls the digital ramp generator in its present state. See the Digital Ramp Generator (DRG) section for more details. If not using a digital ramp generator, connect this pin to Logic 0.
67	SDIO	I/O	Serial Data Input/Output. Digital input/output (active high). This pin can be either unidirectional or bidirectional (default), depending on the configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional mode, it is an input only.
68	SDO	O	Serial Data Output. Digital output (active high). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write, falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the AD9910 use the rising edge. Readback operations from the AD9910 use the falling edge.
70	$\overline{CS}$	I	Chip Select. Digital input (active low). This pin allows the AD9910 to operate on a common serial bus for the control data path. Bringing this pin low enables the AD9910 to detect serial clock rising/falling edges. Bringing this pin high causes the AD9910 to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). This pin can be used when a serial I/O communication cycle fails (see the I/O_RESET—Input/Output Reset section for details). When not used, connect this pin to ground.
80	$\overline{IOUT}$	O	Open-Drain DAC Complementary Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
81	IOUT	O	Open-Drain DAC Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input. When the internal oscillator is engaged, this pin can be driven by either an external oscillator or connected to a crystal. See the REF_CLK/ Overview section for more details.
91	$\overline{REF\_CLK}$	I	Reference Clock Input. Analog input. See the REF_CLK/ Overview section for more details.
94	REFCLK_OUT	O	Crystal Output. Analog output. See the REF_CLK/ Overview section for more details.
95	XTAL_SEL	I	Crystal Select (1.8 V Logic). Analog input (active high). Driving the XTAL_SEL pin high, the AVDD (1.8V) pin enables the internal oscillator to be used with a crystal resonator. If unused, connect it to AGND.
EPAD	Exposed Paddle (EPAD)		The EPAD should be soldered to ground.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

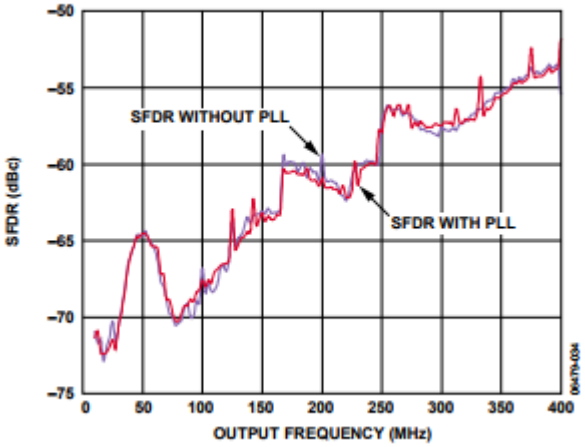


Figure 6. Wideband SFDR vs. Output Frequency (PLL with Reference Clock = 15.625 MHz × 64)

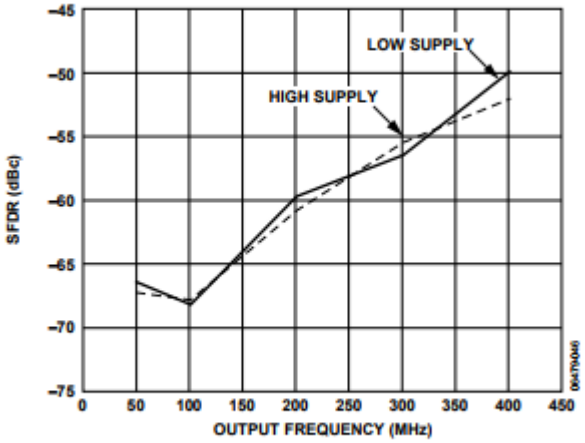


Figure 7. Wideband SFDR vs. Output Frequency and Supply (±5%), REFCLK = 1 GHz

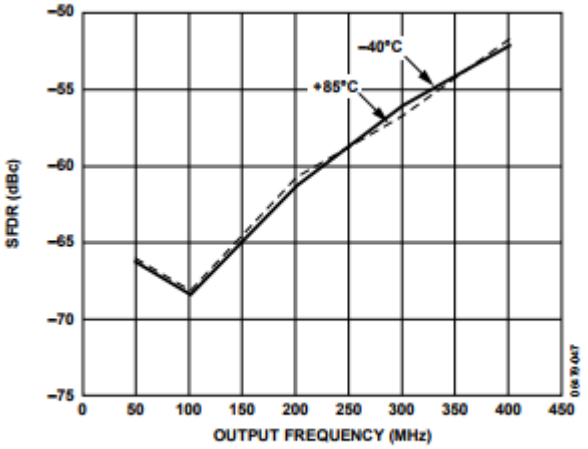


Figure 8. Wideband SFDR vs. Output Frequency and Temperature, REFCLK = 1 GHz

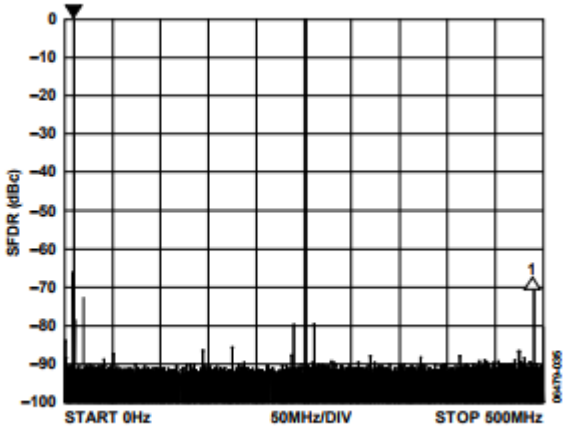


Figure 9. Wideband SFDR at 10 MHz, REFCLK = 1 GHz

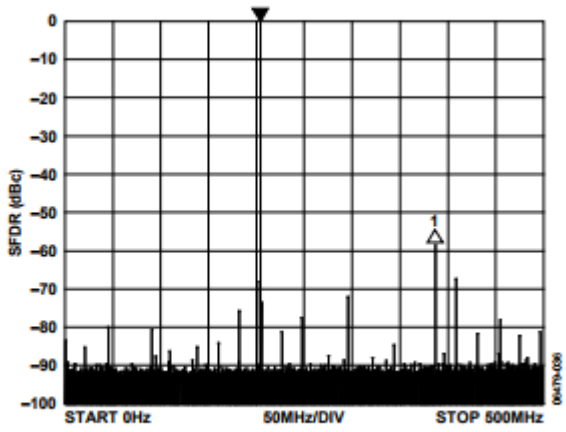


Figure 10. Wideband SFDR at 204 MHz, REFCLK = 1 GHz

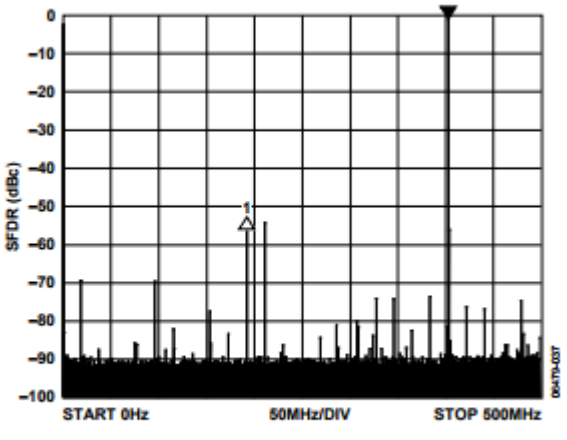


Figure 11. Wideband SFDR at 403 MHz, REFCLK = 1 GHz

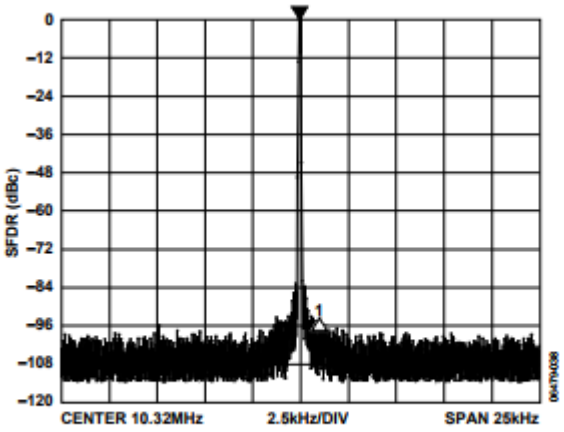


Figure 12. Narrow-Band SFDR at 10.32 MHz, REFCLK = 1 GHz

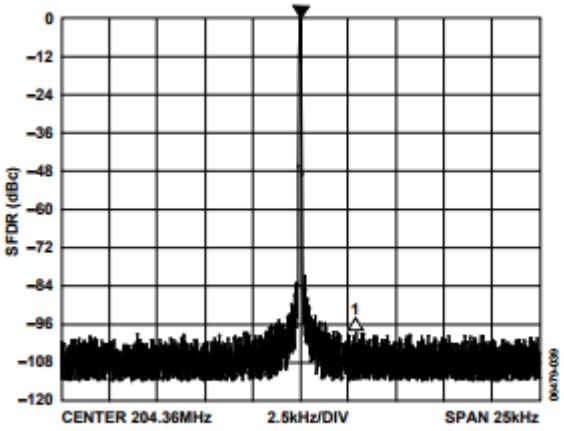


Figure 13. Narrow-Band SFDR at 204.36 MHz, REFCLK = 1 GHz

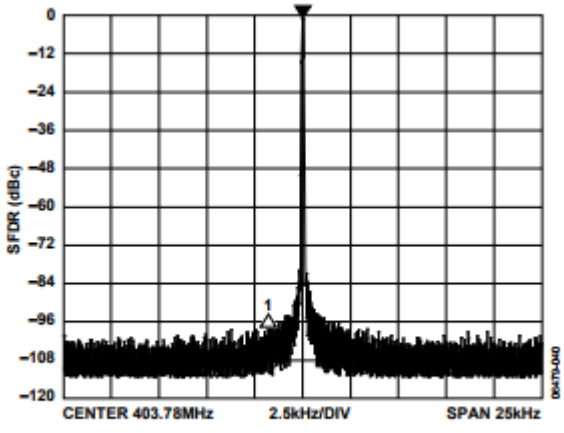


Figure 14. Narrow-Band SFDR at 403.78 MHz, REFCLK = 1 GHz

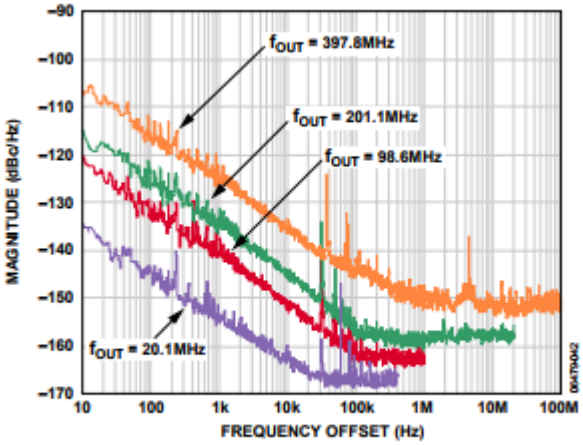


Figure 15. Residual Phase Noise Plot, 1 GHz Operation with PLL Disabled