LMV33x-N / LMV393-N General-Purpose, Low-Voltage, Tiny Pack Comparators

1 Features

- (For 5-V Supply, Typical Unless Otherwise Noted)
- Ensured 2.7-V and 5-V Performance
- Industrial Temperature Range −40°C to 85°C
- Low Supply Current 60 µA/Channel
- Input Common Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV
- Propagation Delay 200 ns
- Space-Saving 5-Pin SC70 and 5-Pin SOT23 Packages

2 Applications

- Mobile Communications
- Notebooks and PDAs
- Battery-Powered Electronics
- General-Purpose Portable Devices
- General-Purpose, Low-Voltage Applications

3 Description

The LMV393-N and LMV339-N are low-voltage (2.7 to 5 V) versions of the dual and quad comparators, LM393/339, which are specified at 5 to 30 V. The LMV331-N is the single version, which is available in space-saving, 5-pin SC70 and 5-pin SOT23 packages. The 5-pin SC70 is approximately half the size of the 5-pin SOT23.

The LMV393-N is available in 8-pin SOIC and VSSOP packages. The LMV339-N is available in 14-pin SOIC and TSSOP packages.

The LMV331-N/393-N/339-N is the most cost-effective solution where space, low voltage, low power, and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

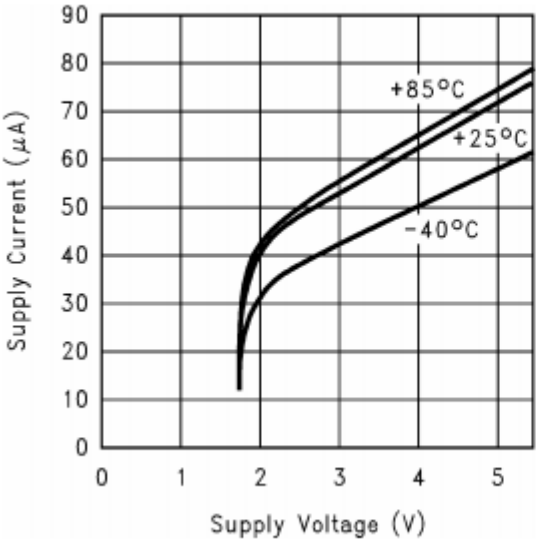
The chips are built with TI's advanced Submicron Silicon-Gate BiCMOS process. The LMV331-N/393-N/339-N have bipolar input and output stages for improved noise performance.

Table 1. Device Information(1)

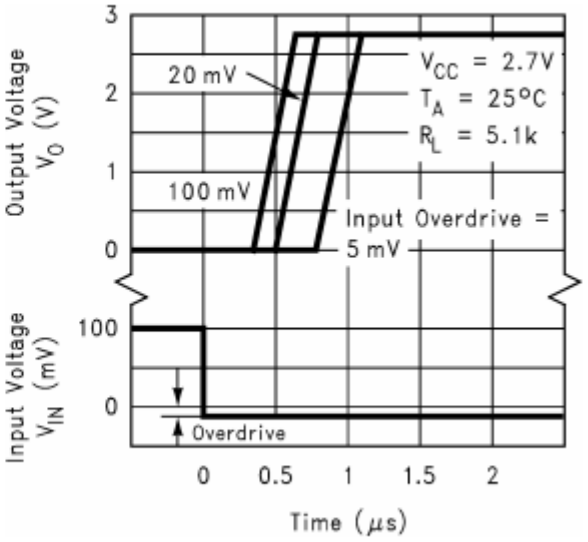
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV331-N	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.6 mm
LMV339-N	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LMV393-N	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Low Supply Current

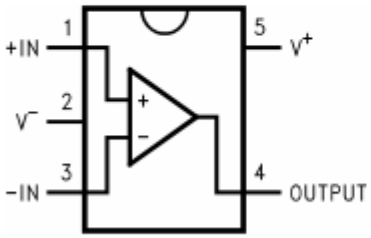


Fast Response Time

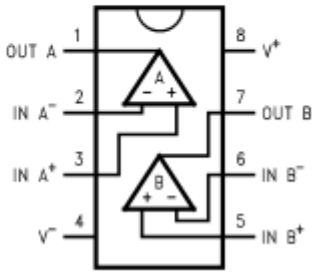


5 Pin Configuration and Functions

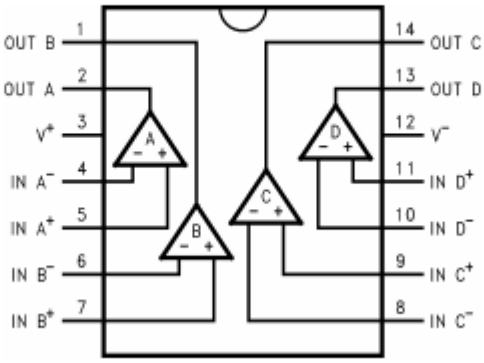
DCK and DBV Package
5-Pin SC70 / SOT23
Top View



D and DGK Package
8-Pin SOIC / VSSOP
Top View



D and PW Package
14-Pin SOIC / TSSOP
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	LMV331-N DVB,DCK	LMV393-N D,DGK	LMV339-N PW		
+IN	1	-	-	I	Noninverting input
+IN A	-	3	5	I	Noninverting input, channel A
+IN B	-	5	7	I	Noninverting input, channel B
+IN C	-	-	9	I	Noninverting input, channel C
+IN D	-	-	11	I	Noninverting input, channel D
-IN	3	-	-	I	Inverting input
-IN A	-	2	4	I	Inverting input, channel A
-IN B	-	6	6	I	Inverting input, channel B
-IN C	-	-	8	I	Inverting input, channel C
-IN D	-	-	10	I	Inverting input, channel D
OUT	4	-	-	O	Output
OUT A	-	1	2	O	Output, channel A
OUT B	-	7	1	O	Output, channel B
OUT C	-	-	14	O	Output, channel C
OUT D	-	-	13	O	Output, channel D
V+	5	8	3	P	Positive (highest) power supply
V-	2	4	12	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Differential Input Voltage		±Supply Voltage	
Voltage on any pin (referred to V^- pin)		5.5	V
Soldering Information			
Infrared or Convection (20 sec)		235	°C
Junction Temperature (3)		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±800	V
	Machine model	±120	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage	2.7	5	V
Temperature Range (2)	−40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC(1)	LMV331-N		LMV339-N		LMV393-N		UNIT
	DCK	DBV	D	PW	D	DGK	
	5 PINS	5 PINS	14 PINS	14 PINS	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	478	265	145	155	190	23	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage			1.7	7	mV
TCV_{OS}	Input Offset Voltage Average Drift	At the temperature extremes		5		µV/°C

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

2.7-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_B	Input Bias Current			10	250	nA
		At the temperature extremes			400	
I_{OS}	Input Offset Current			5	50	nA
		At the temperature extremes			150	
V_{CM}	Input Voltage Range			−0.1		V
				2.0		V
V_{SAT}	Saturation Voltage	I_{SINK} ≤ 1 mA		120		mV
I_O	Output Sink Current	V_O ≤ 1.5V	5	23		mA
I_S	Supply Current	LMV331-N		40	100	µA
		LMV393-N Both Comparators		70	140	µA
		LMV339-N All four Comparators		140	200	µA
	Output Leakage Current			.003		µA
		At the temperature extremes			1	

6.6 2.7-V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7 V, R_L = 5.1 kΩ, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		1000		ns
		Input Overdrive = 100 mV		350		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		500		ns
		Input Overdrive = 100 mV		400		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.7 5-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage			1.7	7	mV
		At the temperature extremes			9	
TCV_{OS}	Input Offset Voltage Average Drift			5		µV/°C
I_B	Input Bias Current			25	250	nA
		At the temperature extremes			400	
I_{OS}	Input Offset Current			2	50	nA
		At the temperature extremes			150	
V_{CM}	Input Voltage Range			−0.1		V
				4.2		V
A_V	Voltage Gain		20	50		V/mV

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

5-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{sat}	Saturation Voltage	$I_{SINK} \le 4$ mA		200	400	mV
		At the temperature extremes			700	
I_O	Output Sink Current	$V_O \le 1.5$V		84	10	mA
I_S	Supply Current	LMV331-N		60	120	µA
		At the temperature extremes			150	
		LMV393-N Both Comparators		100	200	µA
		At the temperature extremes			250	
		LMV339-N All four Comparators		170	300	µA
		At the temperature extremes			350	
	Output Leakage Current			.003		µA
		At the temperature extremes			1	

6.8 5-V AC Electrical Characteristics

T_J = 25°C, V^+ = 5 V, R_L = 5.1 kΩ, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		600		ns
		Input Overdrive = 100 mV		200		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		450		ns
		Input Overdrive = 100 mV		300		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

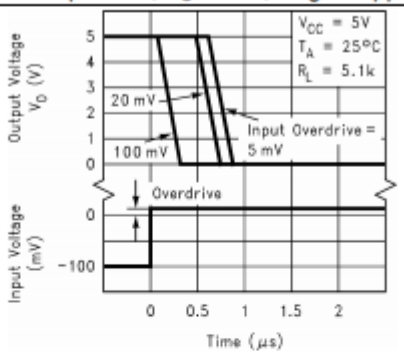


Figure 7. Response Time for Input Overdrive Positive Transition

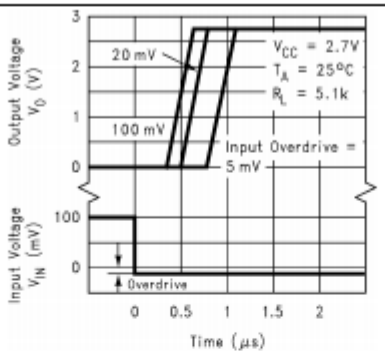


Figure 8. Response Time vs. Input Overdrive Negative Transition

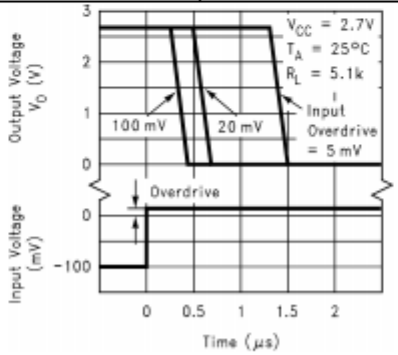


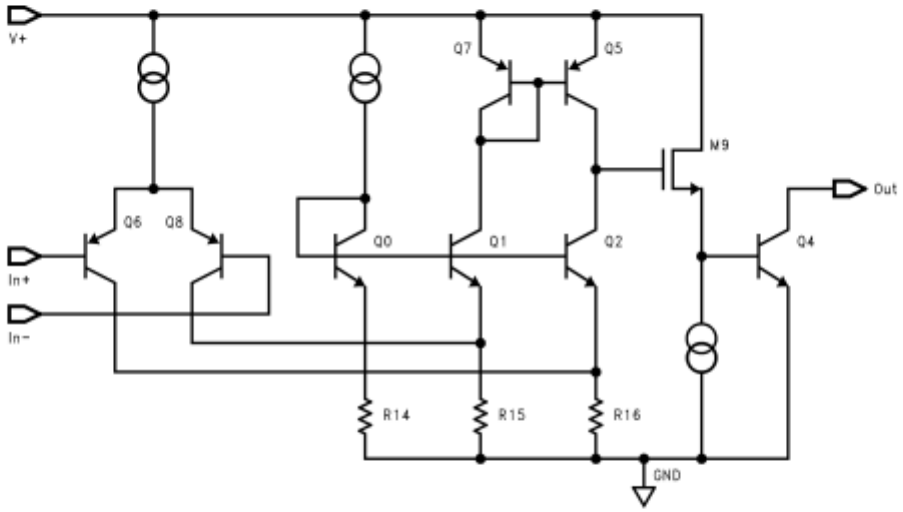
Figure 9. Response Time for Input Overdrive Positive Transition

7 Detailed Description

7.1 Overview

The LMV331-N/393-N/339-N comparators features a supply voltage range of 2.7 V to 5 V with a low supply current of 55 µA/channel with propagation delays as low as 200ns. They are avaialble in small, space-saving packages, which makes these comparators versatile for use in a wide range of applications, from portable to industrial. The open collector output configuration allows the device to be used in wired-OR configurations, such as a window comparators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Open Collector Output

The output of the LMV331-N/393-N/339-N series is the uncommitted collector of a grounded-emitter NPN output transistor, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted V+ supply voltage range. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331-N/393-N/339-N the pull-up resistor should range between 1 k to 10 kΩ.

7.3.2 Ground Sensing Input

The LMV331-N/393-N/339-N has a typical input common mode voltage range of −0.1V below the ground to 0.8V below Vcc.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output.

The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input.

The output is LOW when the voltage on the non-inverting (+IN) input is less than the inverting (-IN) input.

The inverting input (-IN) is also commonly referred to as the "reference" or "V_{REF}" input.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator

The comparator compares the input voltage (V_{IN}) at the non-inverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF}, the output voltage (V_O) is at the saturation voltage. On the other hand, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is at V_{CC}.

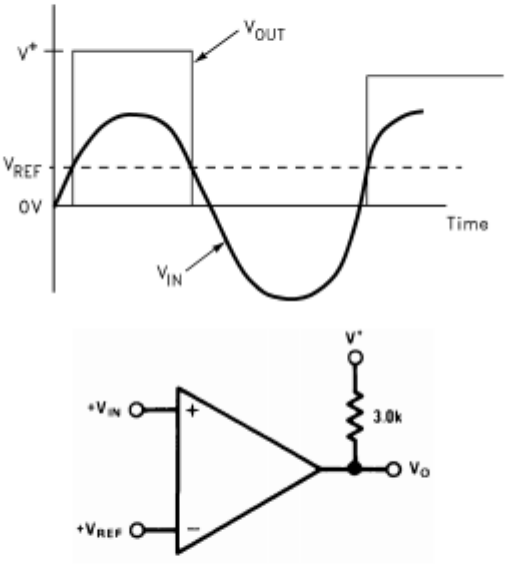


Figure 10. Basic Comparator

8.1.2 Comparator With Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by the addition of hysteresis or positive feedback.

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator. When V_{in} at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1//R_3$ in series with R_2. The lower input trip voltage V_{a1} is defined as:

$$V_{a_1} = \frac{V_{CC}\ R_2}{(R_1 \,||\, R_3) + R_2} \tag{1}$$

When V_{in} is greater than V_a ($V_{in} > V_a$), the output voltage is low very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{a2} is defined as:

$$V_{a2} = \frac{V_{CC}\,(R_2 // R_3)}{R_1 + (R_2 // R_3)} \tag{2}$$

Application Information (continued)

The total hysteresis provided by the network is defined as:

$$\Delta V_a = V_{a1} - V_{a2} \quad (3)$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL\text{-}UP} << R_{LOAD} \quad (4)$$

and $R_1 > R_{PULL\text{-}UP}$. (5)

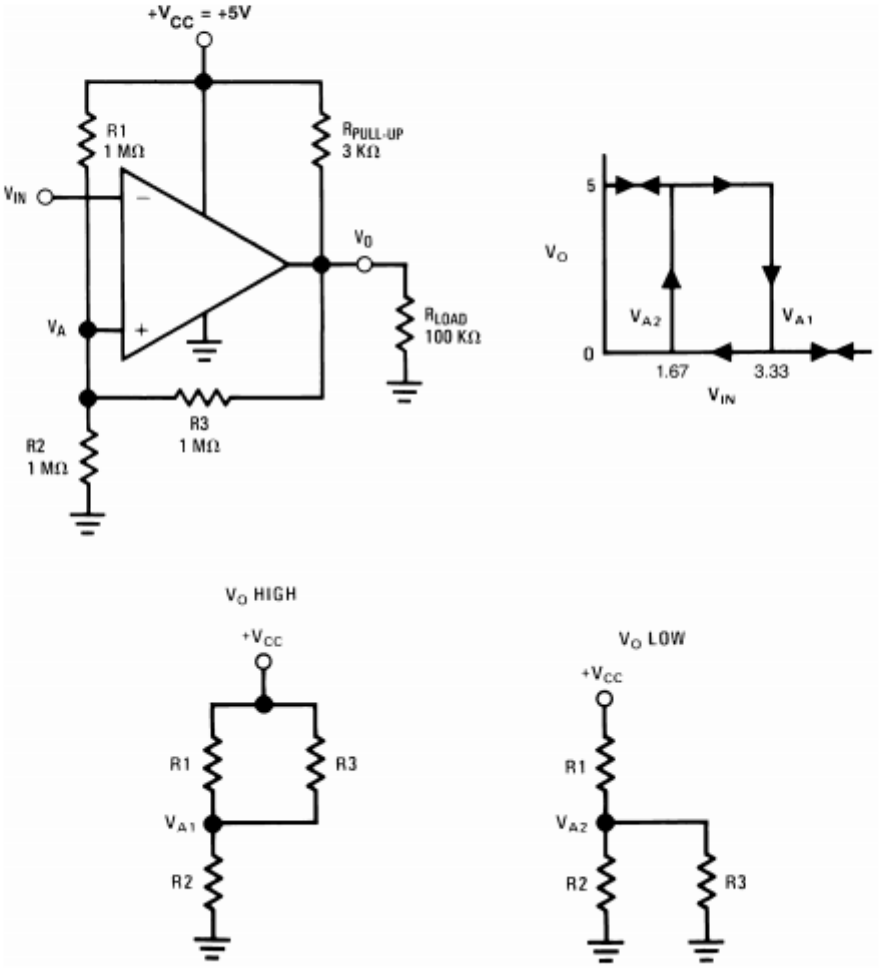


Figure 11. Inverting Comparator With Hysteresis

8.1.2.1.1 Non-inverting Comparator With Hysteresis

Non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by:

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2} \quad (6)$$

When V_{in} is high, the output is also high. To make the comparator switch back to its low state, V_{in} must equal V_{ref} before V_A will again equal V_{ref}. V_{in} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (7)$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

Application Information (continued)

$$\Delta V_{in} = V_{CC} R_1 / R_2 \quad (8)$$

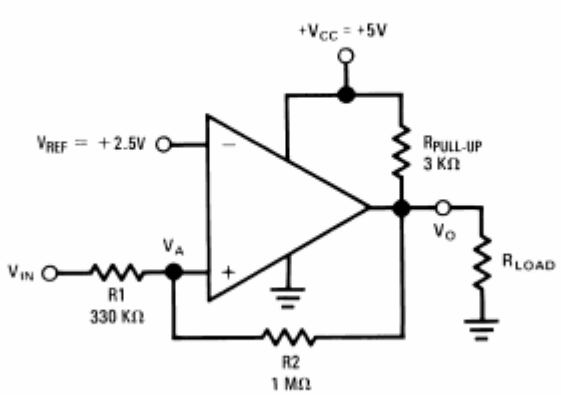


Figure 12. Noninverting Comparator With Hystersis

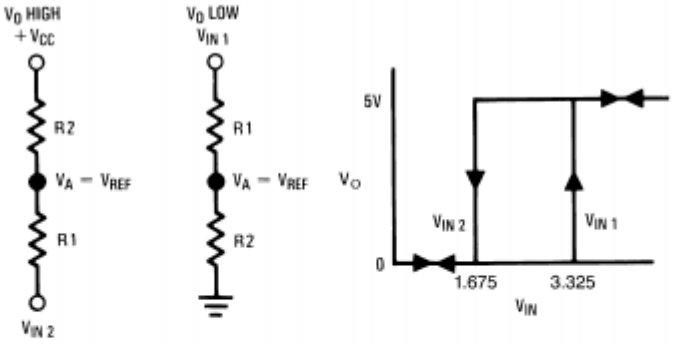


Figure 13. Hysteresis Threshold Points

8.1.3 ORing the Output

By the inherit nature of an open-collector comparator, the outputs of several comparators can be tied together with a shared pull-up resistor to V_{CC}. If one or more of the comparators outputs goes low, the output V_O will go low.

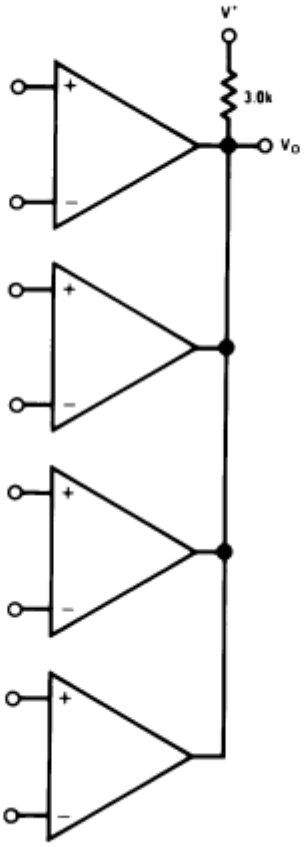


Figure 14. ORing the Outputs

8.1.4 Driving CMOS and TTL

The output of the comparator is capable of driving CMOS and TTL Logic circuits. The pull-up resistor may be pulled-up to any voltage equal to, or less than the supply voltage on V+. However, it must not be pulled-up to a voltage higher than V+.

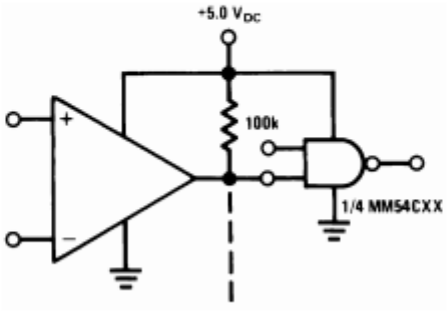


Figure 15. Driving CMOS

8.1.6 OR Gates

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to V_{cc}, thereby reducing the reference voltage.

A logic 1 at any of the inputs will produce a logic 1 at the output.

Application Information (continued)

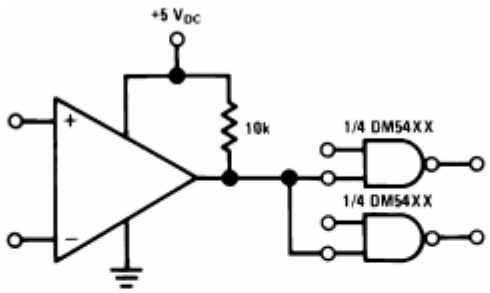


Figure 16. Driving TTL

8.1.5 AND Gates

The comparator can be used as three input AND gate. The operation of the gate is as follows:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a 0 equal to ground and a 1 equal to 5 V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

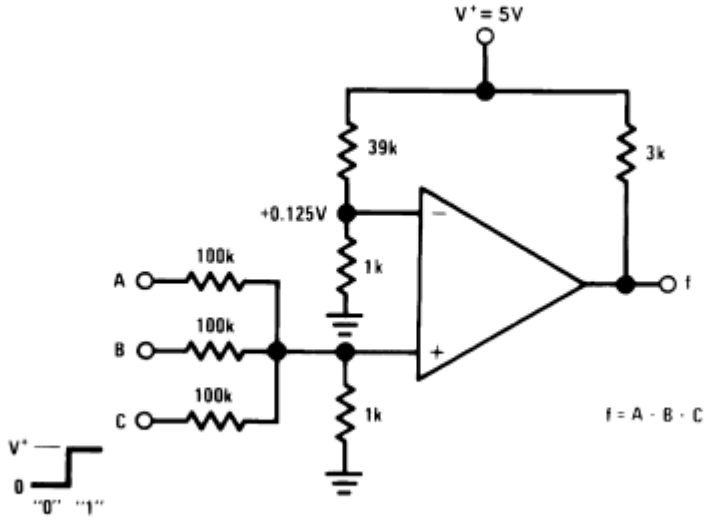


Figure 17. AND Gate