

IR2112(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description

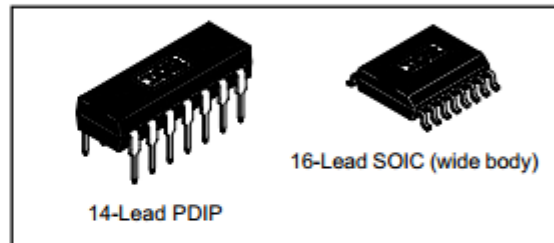
The IR2112(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic.

The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

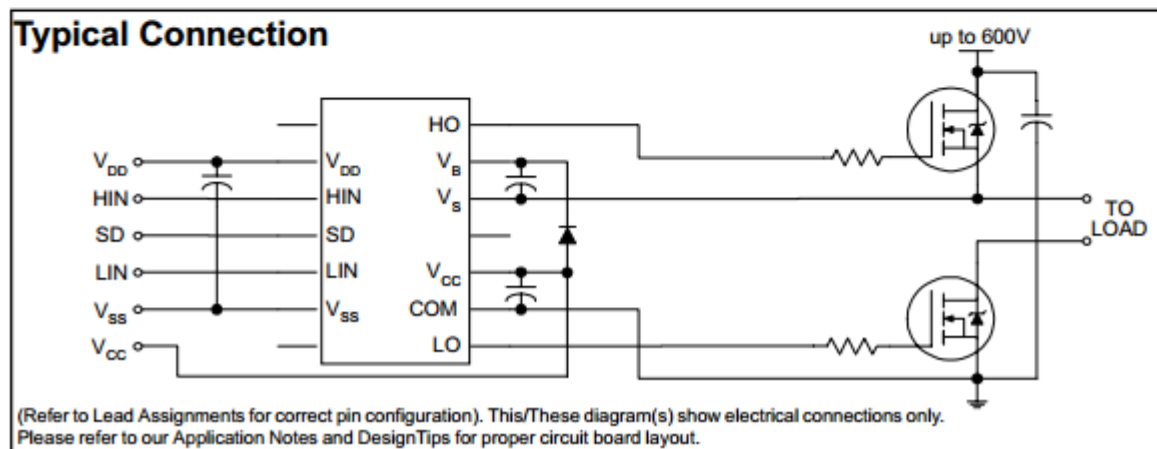
Product Summary

V_{OFFSET}	600V max.
$I_{\text{O}+/-}$	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{\text{on/off}}$ (typ.)	125 & 105 ns
Delay Matching	30 ns

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units	
V _B	High Side Floating Supply Voltage	-0.3	625	V	
V _S	High Side Floating Supply Offset Voltage	V _B - 25	V _B + 0.3		
V _{HO}	High Side Floating Output Voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low Side Fixed Supply Voltage	-0.3	25		
V _{LO}	Low Side Output Voltage	-0.3	V _{CC} + 0.3		
V _{DD}	Logic Supply Voltage	-0.3	V _{SS} + 25		
V _{SS}	Logic Supply Offset Voltage	V _{CC} - 25	V _{CC} + 0.3		
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3		
dV _S /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50		V/ns
P _D	Package Power Dissipation @ T _A ≤ +25°C	(14 Lead DIP)	—	1.6	W
		(16 Lead SOIC)	—	1.25	
R _{THJA}	Thermal Resistance, Junction to Ambient	(14 Lead DIP)	—	75	°C/W
		(16 Lead SOIC)	—	100	
T _J	Junction Temperature	—	150	°C	
T _S	Storage Temperature	-55	150		
T _L	Lead Temperature (Soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V _B	High Side Floating Supply Absolute Voltage	V _S + 10	V _S + 20	V
V _S	High Side Floating Supply Offset Voltage	Note 1	600	
V _{HO}	High Side Floating Output Voltage	V _S	V _B	
V _{CC}	Low Side Fixed Supply Voltage	10	20	
V _{LO}	Low Side Output Voltage	0	V _{CC}	
V _{DD}	Logic Supply Voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS}	V _{DD}	
T _A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to -V_{DD}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

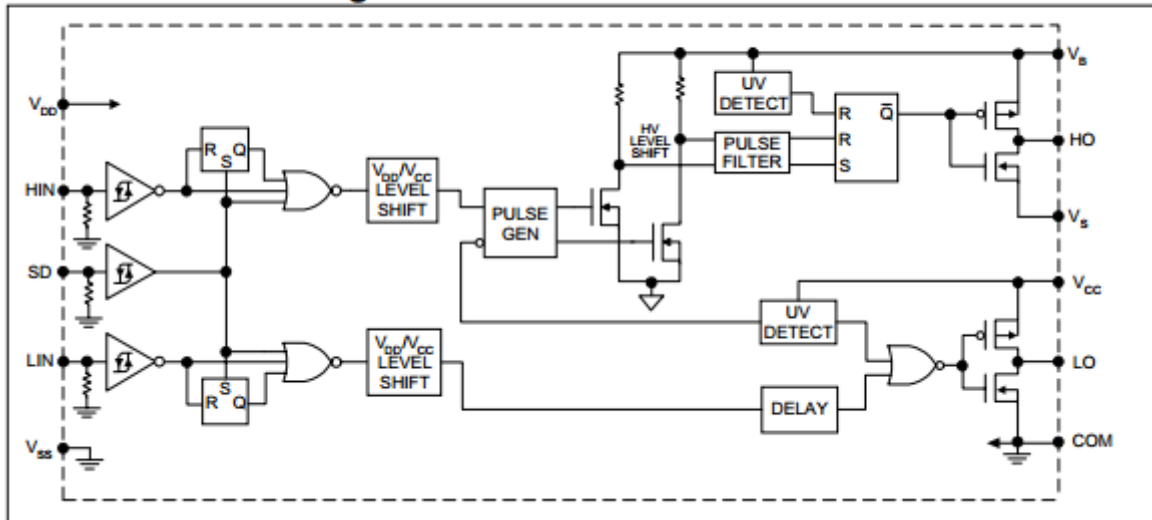
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t _{on}	Turn-On Propagation Delay	7	—	125	180	ns	V _S = 0V
t _{off}	Turn-Off Propagation Delay	8	—	105	160		V _S = 600V
t _{sd}	Shutdown Propagation Delay	9	—	105	160		V _S = 600V
t _r	Turn-On Rise Time	10	—	80	130		
t _f	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0	V	
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	14	—	—	100	mV	$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	15	—	—	100	mV	$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	16	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	25	60		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	80	180		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	2.0	5.0		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0	V	$V_{IN} = 0V$
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
I_{O+}	Output High Short Circuit Pulsed Current	26	200	250	—	mA	$V_O = 0V, V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	27	420	500	—		$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$

Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

<p>14 Lead PDIP IR2112</p>	<p>16 Lead SOIC (Wide Body) IR2112S</p>
<p>14 Lead PDIP w/o lead 4 IR2112-1</p>	<p>14 Lead PDIP w/o leads 4 & 5 IR2112-2</p>
Part Number	

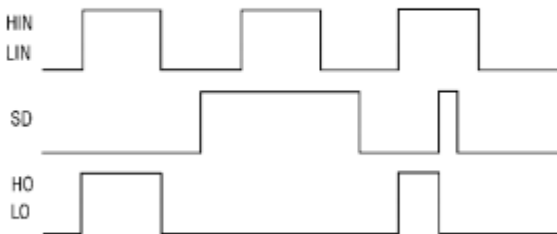


Figure 1. Input/Output Timing Diagram

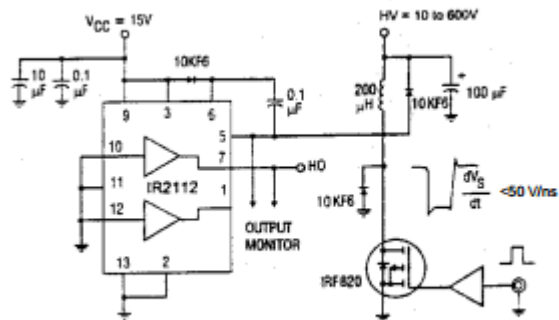


Figure 2. Floating Supply Voltage Transient Test Circuit

